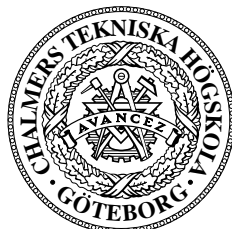


Coulomb blockade effects in anodised niobium nanostructures

(Coulomb-blockad-effekter
i anodiserade Nb-nanostrukturer)

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Abstract

Niobium thin film nanostructures were fabricated using electron beam lithography and a liftoff process involving a four layer resist system. Wires having micrometres in length and below 200 nm in width were deposited on an insulating substrate and subsequently thinned by anodisation. The resistance of the wires was monitored in situ and could be trimmed by controlling the anodisation voltage and time. The method appears appropriate for the fabrication of very small resistors for use as biasing resistors for single electron devices. Transport properties of these resistors were measured at millikelvin temperatures. They had nonlinear current-voltage characteristics around zero bias and showed a transition from superconducting to insulating behaviour. Analysis of the offset voltage showed that a Coulomb blockade set in when the sheet resistance of the films exceeded the superconducting quantum resistance $\approx 6.45 \text{ k}\Omega$.

Samples in a single electron transistor-like geometry with two variable thickness weak links were made by combined angular evaporation of niobium and anodisation. Overlapping gate electrodes were deposited on these samples. The drain-source current-voltage characteristics could be modulated by the gate voltage, giving a response typical for a system of multiple ultrasmall tunnel junctions.

Keywords: niobium, columbium, anodisation, nanofabrication, Coulomb blockade, superconductor-insulator transition

Sammanfattning

Tunnfilms-nanostrukturer av niob tillverkades med hjälp av elektronstråle-litografi och en liftoff-process som använder sig av ett fyrlagers-resistsystem. Ledningar av några mikrometers längd och en bredd mindre än 200 nm deponerades på ett isolerande substrat och förtunnades sedan genom anodisering. Ledningarnas resistans mättes kontinuerligt under anodiseringen och kunde trimmas genom att kontrollera anodiseringsspänningen och -tiden. Metoden förefaller lämpad för tillverkning av mycket små resistorer som behövs som biaseringsresistorer för en-elektron-komponenter. Transportegenskaperna hos resistorerna mättes vid millikelvin-temperaturer, som visade ickelinjära ström-spännings-karakteristika vid låga spänningar och en övergång från supraledande till isolerande uppförande. Analys av förskjutningsspänningen gav att en Coulomb-blockad framträdde när filmernas ytmotstånd överskred den supraledande kvantresistansen $\approx 6.45 \text{ k}\Omega$.

Prover liknande enkelelektron-transistorer med två svaga länkar skapades genom kombinerad skuggförångning av niob och anodisering. En överlappande grindelektrod deponerades på dessa prover. Provernas ström-spännings-karakteristika kunde påverkas av grindspänningen, och de resulterande kurvorna liknar dem som fås i system av många ultrasmå tunnelövergångar.

Nyckelord: niob, anodisering, nanofabrikation, Coulomb-blockad, supraleddare-isolator-övergång

Contents

List of Figures	7
Preface	9
1 Introduction, background	11
1.1 Tunnelling and superconductivity	11
1.1.1 Tunnelling	11
1.1.2 Superconductivity	13
1.1.3 Josephson effects	14
1.2 Charging effects	14
1.2.1 Charging effects in very small tunnel junctions	14
1.2.2 Charging effects in granular films	16
1.3 Three terminal charging effect devices	17
1.4 The need for smaller resistors	18
1.4.1 Coulomb blockade and electromagnetic environment	18
1.4.2 Resistors in single electronics	19
1.5 Superconductor-insulator transition in thin films	20
1.6 Anodisation of niobium	20
1.6.1 Electrochemistry of niobium and its oxides	21
1.6.2 Micro- and nanofabrication by anodisation	22
2 Nanofabrication and microanodisation	25
2.1 Substrate and carrier system	25
2.2 A niobium liftoff nanofabrication process	27
2.2.1 Pattern design and compilation	28
2.2.2 Four layer resist system	28
2.2.3 Pattern definition with electron beam lithography	29
2.2.4 Pattern transfer	31
2.3 Microanodisation of niobium	35
2.3.1 Experimental setup and procedures	35
2.3.2 Anodisation dynamics	39
2.4 Top gate electrodes	40
2.4.1 Preparation	41
2.4.2 Electrical properties	41

3	Electronic transport in anodised niobium nanostructures	43
3.1	Measurement setup and procedure	43
3.1.1	Cryogenics	43
3.1.2	Shielding and Filtering	44
3.1.3	Measurement electronics	44
3.2	Resistor samples	44
3.2.1	Sample geometry	45
3.2.2	Current-voltage characteristics	45
3.2.3	Measuring the Coulomb blockade: the offset voltage . . .	48
3.2.4	Onset of the CB: a superconductor-insulator transistion .	49
3.3	Samples in SET-like geometry	51
3.3.1	Current-voltage characteristics	51
3.3.2	Control curves	52
3.3.3	Gate modulated IVC	53
3.3.4	Temperature dependence	53
4	Conclusion	61
4.1	Status quo	61
4.2	Directions for future research	62
	Bibliography	63
A	Symbols and notation	73
B	Glossary and abbreviations	75
C	Recipes	81
C.1	Photomask making	81
C.2	Gold pad photolithography (carrier chips)	82
C.3	Four layer resist preparation	82
C.4	Four layer resist exposure	83
C.5	Four layer resist proximity correction	83
C.6	Four layer resist processing	83
C.7	Anodisation window mask	84
C.8	Electrolyte for Nb anodisation	84
C.9	Two layer resist for high resolution EBL	84
C.10	Ti dot patterns (etch mask for IBE) on II-VI semiconductors . .	84
C.11	Ar ⁺ ion beam milling of II-VI semiconductor quantum dots . . .	85
C.12	Chemical etching of II-VI semiconductor quantum dots	85

List of Figures

1.1	Tunnelling between metallic conductors	12
1.2	Symbol for ultrasmall junction	15
1.3	Overlap junction	15
1.4	Single electron transistor	17
1.5	Anodisation setup for resistor fabrication.	22
2.1	Fabrication process: overview	26
2.2	Etch vs. liftoff process	27
2.3	Four layer resist processing	29
2.4	Four layer resist mask after oxygen etching	32
2.5	Contamination of large Nb areas	33
2.6	Technique for fabrication of samples in SET-like geometry	34
2.7	Variable thickness weak links in Nb wire	35
2.8	Experimental setup for Nb microanodisation	36
2.9	Anodisation mask, optical micrograph	36
2.10	Anodisation control programme user interface	38
2.11	Anodisation process	39
2.12	Long-time anodisation process	40
2.13	Top gate on anodised double weak link structure	41
2.14	Top gate electrical leakage	42
3.1	Current-voltage characteristics for resistor samples	45
3.2	Resistor IVC: magnetic field dependence; switching	46
3.3	Zero bias differential resistance: temperature dependence	47
3.4	Definition of V_{off}^0	48
3.5	Onset of Coulomb blockade in resistor samples	50
3.6	Coulomb blockade in weak links sample	55
3.7	Magnetic field dependence of conductance extrema in weak links sample	56
3.8	Control curves for weak links sample	57
3.9	Gate modulated I - V characteristics of weak links sample	58
3.10	Gate modulation above 1 K	59
3.11	Temperature dependence of gate modulation	60

Preface

*‘I have thought about some of the problems
of building electric circuits on a small scale,
and the problem of resistance is serious.’
(Richard P. Feynman, 1959[1])*

Before we start with any scientific stuff, let me thank some people who have contributed a lot to this thesis, or to the fact that I could write it here. First of all Tord Claeson, who gave me the chance to start working in his group. Then of course Bengt Nilsson, for many good suggestions and most of all for keeping the SnL up and running so smoothly that we hardly know how to spell *dauntajm*. Thanks to all those who keep paperwork from us and make the SnL probably the least bureaucratic nanofabrication facility in the world, especially Ann-Marie Frykestig. Thanks to Staffan Pehrson and Henrik Frederiksen for many small and some really big things they built and serviced. I’m mainly thinking about the Niobium System, of course. Peter Wahlgren also invested a lot of time into that machine. Last but not least Per Delsing and David Haviland, who initiated and supervised this work, and the numerous PhD students, past and present, who helped in one way or another.

A more formal, but nonetheless cordial thankyou to the German Academic Exchange Service DAAD, who financed my first year here ‘im Rahmen des Zweiten Hochschulsonderprogramms’, and to the Commission of the European Communities, who support me presently. This work was part of ESPRIT programme 9005 SETTRON.

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2. Torsten Henning, D. B. Haviland, P. Delsing: *Fabrication of Coulomb blockade elements with an electrolytic anodization process*. Symposium on Single-Electron nanoelectronics, 190th Meeting of the Electrochemical Society (San Antonio, 6–11 October 1996)

3. Torsten Henning, D. B. Haviland, P. Delsing: *Charging effects and superconductivity in anodised niobium nanostructures*. 6th International Superconductive Electronics Conference (Berlin, 25–28 June 1997)

and at the Spring Meetings of the German Physical Society. A paper has been submitted:

- 4 Torsten Henning, D. B. Haviland, P. Delsing: *Coulomb blockade effects in anodised niobium nanostructures*. submitted to Superconductor Science and Technology 1997-05-09

The International system of Units is used exclusively throughout this work. In questions of style connected with the SI, I follow largely the recommendations of the National Institute of Standards and Technology [2], not so much because I think America is leading in the sound use of units, but because they were so kind to publish their booklet free of charge on the WWW. Appendix A explains the nomenclature used. Making graphic representations of data is a science in itself (and not a question of taste). I recommend the book by Cleveland [3], whose guidelines I tried to follow.

Nanofabrication, like all branches of technology, has developed its own set of acronyms and abbreviations. I have collected as much jargon as possible in a glossary that you will find as appendix B.

Appendix C lists in detail all the processes that were developed or used in the course of this work. Recipes are always subject to change, and the appendix reflects the latest state of the art, so samples described in this thesis may have been fabricated by a process with different parameters.

Appendix omitted from the WWW edition: This thesis is concluded by a seemingly unrelated appendix on the lateral nanostructuring of II-VI semiconductor heterostructures. Well, not so unrelated, because there is a lot of general nanofabrication know-how involved that is common to the niobium nanostructures treated in the main part, and to the quantum dots mentioned in this appendix. This project was initiated and is coordinated by Peter Klar, PhD by now, of UEA Norwich. Thanks to him for giving me the opportunity to do even more useful things with all the nice equipment here. And once again to Bengt Nilsson for working countless overtime hours and repairing the JEOL just when we needed it most.

Chapter 1

Introduction, background

This chapter is intended to give a brief introduction to some of the basic phenomena and concepts relevant for the work covered in this report. For a more thorough introduction, there is a lot of reference material and textbooks on tunnelling, superconductivity [4], and charging effects [5, 6, 7]. Reference material on niobium and its anodisation is quoted in the respective sections below.

1.1 Tunnelling and superconductivity

Tunnelling and superconductivity are two quantum phenomena that are observed in transport measurements.

1.1.1 Tunnelling

Tunnelling is a transport mechanism that can only be understood in terms of quantum mechanics. Consider a conduction electron with energy E near the Fermi surface in a region that we call ‘left electrode’, and an adjacent region called ‘barrier’ where the conduction band edge lies at a higher energy. On the other side of the barrier we have the ‘right electrode’. Even if the Fermi energy in the right electrode is different from that in the left electrode, classical physics would prohibit the transmission of the electron. Quantum mechanics, however, predicts a nonvanishing transmission through the barrier as long as it is finite in height (energetic) and width (in real space).

A voltage applied between left and right electrode results in a current flow. For small voltages, the current-voltage characteristics are linear and define a tunnelling resistance R_T . Tunnelling processes are classified as elastic, if the energy of the tunnelling particle is conserved, or inelastic. In the latter case, dissipation occurs through excitations in the barrier, the electrodes, or the electrode-barrier interfaces. Figure 1.1 is a schematic representation of the tunnelling between two metallic conductors.

Two examples of systems showing tunnelling are metallic tips showing field

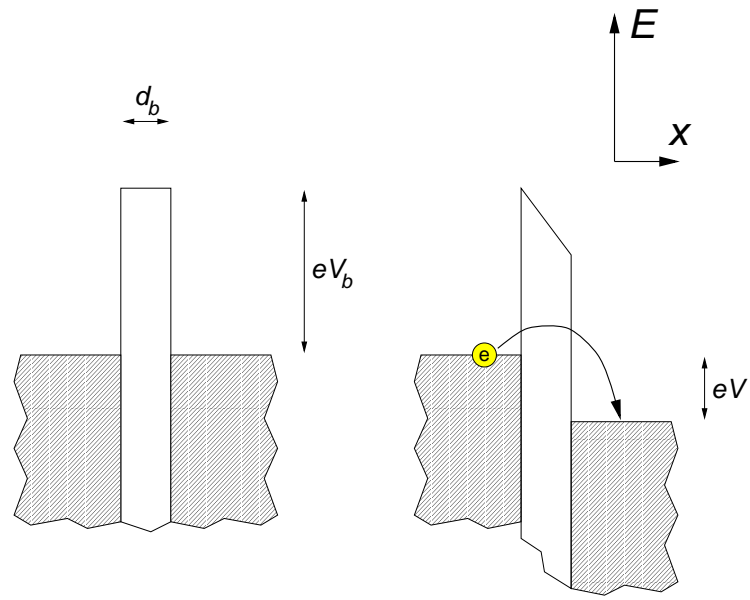


Figure 1.1: Schematic representation of the tunnelling between two metallic conductors separated by a barrier of height eV_b and width d_b . In the right picture, the junction is biased with a voltage V , favouring (inelastic) tunnelling of electrons from the left to the right electrode.

emission, and structures with a thin insulator separating two conductors. In the first case, the ‘left electrode’ is the metal tip, and the barrier is created by the work function, i.e. the energy needed to move an electron from the conductor to infinity. An electric field tilts the vacuum level, resulting in a triangular shaped barrier that allows the emission of electrons into vacuum (‘right electrode’). This effect is not only of historical interest as an early verification of quantum mechanics (observed by Lilienfeld in 1922 and explained by Fowler and Nordheim in 1928), it is also of technological importance as the working principle of advanced electron guns in electron beam lithography machines. The second example, conductor-insulator-conductor structures in different varieties, is the main subject of this report.

1.1.2 Superconductivity

Below a critical temperature T_c and critical magnetic field H_c , certain materials are in a thermodynamic state called the ‘superconducting state’. It manifests itself in a number of effects. The first effect discovered was the vanishing of the electrical resistance, which gave the phenomenon its name [8]. Of at least equal importance is the fact that superconductors expel magnetic fields, the Meissner-Ochsenfeld effect [9].

We will in this report only be dealing with so-called ‘low temperature’ superconductors. These materials are rather well understood theoretically, much better than the ‘high temperature’ superconductors that were discovered just more than a decade ago [10]. A microscopic theory that is well confirmed experimentally is that of Bardeen, Cooper and Schrieffer (BCS, [11]). Pairs of electrons in time reversed states (opposite spin and wave vector) interact by exchange of virtual phonons, leading to an attractive interaction and the formation of so-called ‘Cooper pairs’. A collective effect results in the formation of a ground state that has a lower energy than the Fermi sphere and a gap in the density of states around the Fermi energy. The energetic width of this gap is 2Δ , the energy required to break up a Cooper pair and create an excitation.

The density of states has a singularity at the gap edges. It was measured by Giaever in tunnelling experiments that are a direct verification of the BCS theory.

Characteristic material parameters are the gap (at zero temperature) $\Delta(0)$, the London penetration depth λ , the characteristic length over which a magnetic field drops at the superconductor surface, and the coherence length ξ , over which the Cooper pair density varies. The critical temperature depends on the gap at zero temperature, and the gap energy vanishes at the critical temperature. Niobium is the element with the highest critical temperature (at ambient pressure), $T_c \approx 9.2$ K in bulk, corresponding to a gap of $2\Delta \approx 3$ mV. The gap is reduced in thin films, considerably below 50 nm thickness [12]. The London penetration depth of niobium is $\lambda = 32$ nm [13], and the coherence length $\xi = 39$ nm [13].

1.1.3 Josephson effects

The superconducting condensate is described by a multiparticle wave function with a phase $\phi_i(x, t)$. A tunnel junction with an oxide barrier and superconducting electrodes is one example of a system where two superconducting condensates are more or less strongly coupled. For such systems, Josephson [14] predicted several effects that now summarily bear his name. Important for us is the so-called DC Josephson effect. Between the two superconductors, a supercurrent can flow, that is a current without a voltage drop. The maximally possible supercurrent (Josephson pair current) has the following dependence on the phase difference $\gamma = \phi_r - \phi_l$ [4]:

$$I_c = I_{c0} \sin \gamma. \quad (1.1)$$

The coupling between the superconductors is often expressed in terms of a coupling energy

$$E_J = \frac{\hbar}{2e} I_{c0}. \quad (1.2)$$

1.2 Charging effects

In this section, we will give a brief introduction to the subject of charging energy, proceeding from simple circuits to granular films rather than historically vice versa.

1.2.1 Charging effects in very small tunnel junctions

A metal-insulator-metal tunnel junction has a capacitance C that relates its charge Q to the potential drop V between the electrodes. Not only does the concept of capacitance apply on the submicron length scale, even the approximation as a parallel plate capacitor with capacitance

$$C = \frac{\varepsilon_0 \varepsilon A}{d}, \quad (1.3)$$

with d the thickness of the oxide barrier, works quite well for junctions in the submicrometre size range.

The symbol used for ultrasmall tunnel junctions (see figure 1.2) represents a combination of a tunnelling resistance R_T and a capacitance C . Figure 1.3 shows how such a junction is generally implemented as an overlap junction.

Charging the junction to Q requires an energy

$$E_{ch} = \frac{Q^2}{2C}. \quad (1.4)$$

The charge Q of a junction is a continuous variable, since the (continuous) voltage V can induce any polarisation charge. If the charge carriers are localised on either side of the barrier, tunnelling causes changes of the charge in integer

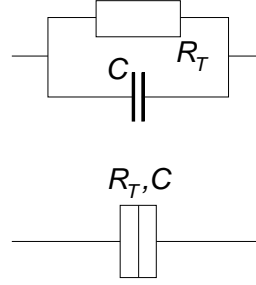
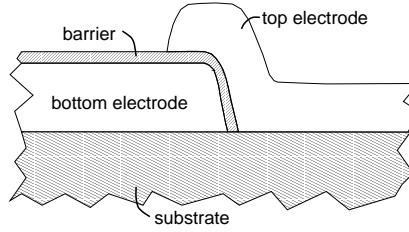


Figure 1.2: Symbol for an ultrasmall tunnel junction (bottom), a combination of the symbols for a tunnelling resistance R_T and a capacitance C in parallel (top).

Figure 1.3: Implementation of an ultrasmall junction as an overlapping junction. The barrier is either formed by oxidising the bottom electrode, e.g. in the case of Al as electrode material, or by depositing a different material and oxidising it, if applicable.



multiples of the elementary charge e . From an argumentation that the characteristic time of charge leakage through the barrier R_TC should be larger than the time associated with the energy change during tunnelling via an uncertainty relation $\Delta\tau\Delta E = \hbar/2$, one arrives at a criterion: charges are localised on either side of the barrier if the tunnelling resistance R_T is large compared to the quantum resistance

$$R_K = \frac{h}{e^2}. \quad (1.5)$$

The index on R_K expresses the current belief [15] that the fraction on the right is exactly the resistance constant that gives the position of plateaux in the quantum Hall or Klitzing effect. This effect is currently being used to realise the resistance standard, and the Klitzing constant has been defined to

$$R_{K-90} \equiv 25812.807 \Omega. \quad (1.6)$$

The characteristic charging energy of a junction is that caused by a single elementary charge,

$$E_C = \frac{e^2}{2C}. \quad (1.7)$$

For a junction with an area of $(100 \text{ nm})^2$ and a 1 nm thick oxide barrier with a dielectric constant of 10, the charging energy corresponds to a temperature of about 1 K. To observe single charge charging effects, the temperature must be lower. Therefore, single electronics, the science of phenomena related to the charging energy and the sometimes continuous and sometimes discrete nature of charge, is today a branch of low temperature physics.

The basis of single electronics is the Coulomb blockade. If an electron tunnels through a junction, its energy changes by $\Delta E = E(Q-e) - E(Q)$. No tunnelling occurs unless ΔE is negative. In an ideal case, this would lead to a linear current-voltage characteristic that is shifted by an offset voltage

$$V_{\text{off}} = (E_C/e)(|V|/V) \quad (1.8)$$

against an Ohmic characteristic.

For a junction with superconducting electrodes, the charge of the Cooper pair $2e$ has to be substituted for e in (1.7).

Kulik and Shekhter calculated in 1975 [16] the current-voltage characteristics for tunnelling through a small grain, something that we nowadays would call a double tunnel junction, with a Coulomb staircase in the asymmetric case. In 1982, Widom et al. [17] pointed out the duality between the Josephson effect and the ‘current bias frequency effect’ that we now know as ‘Bloch oscillations’. Likharev and Zorin worked out the theory of these oscillations in 1985 [18]. Ben-Jacob et al. predicted similar oscillations of the voltage in normalconducting current biased junctions [19]. Soon thereafter, Averin and Likharev published a theory of these SET-oscillations [20]. A three terminal device based on the Coulomb blockade and as a dual analogue to the SQUID was introduced by Likharev as ‘Single electron transistor’ in 1987 [21]. The same year, single electron effects were found experimentally in granular tunnel junctions by Kuzmin and Likharev [22] and in lithographically made junctions by Fulton and Dolan [23].

1.2.2 Charging effects in granular films

Gorter suggested in 1951 [24] that the observed increase of the resistance of thin films at low temperature and low bias might be due to a granular structure of these films and to charging effects impeding the charge transfer between the grains. Neugebauer and Webb [25] treated thin films as a planar array of small islands, between which charge transfer occurred by tunnelling. Taking the charging effects into account, they predicted and measured an Arrhenius type dependence of resistance on temperature (see page 48). The granularity of their samples was demonstrated by TEM imaging.

Giaever and Zeller [26, 27] made Al-AlO_x-Al junctions with Sn particles embedded in the oxide. They found effects of the finite size of the grains, causing a finite spacing of energy levels in the small particle and making it in principle impossible to align Fermi levels in the electrodes and the grains. Assuming a distribution of grain sizes could account for the observed nonlinear current-voltage characteristics, showing what we today call the Coulomb blockade. Since Sn is a superconductor with a critical temperature of 3.7 K (in bulk), above that of Al (1.2 K), Giaever and Zeller could also investigate the superconductivity of very small particles, and claim to have found that superconductivity persisted down to the smallest investigated grain sizes of about 5 nm.

Another experiment with small particles was made by Lambe and Jaklevic [28, 29]: they prepared small particles separated from one electrode by a thin

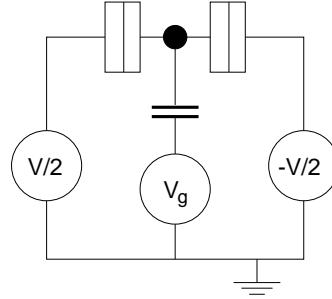


Figure 1.4: Single electron transistor, biased symmetrically with respect to ground.

oxide barrier and from the other electrode by a thick barrier, not transparent for tunnelling electrons and just providing a capacitive coupling to the grains. In modern terms we would call this a parallel coupling of different single electron boxes. They found by capacitance measurements that the grains were charged stepwise with increasing voltage by tunnelling through the thinner barrier, and observed a quantum field effect when they modulated the energy levels in the grains by applying an external electrical field. A quantum mechanical treatment with a charging and a tunnelling Hamiltonian was presented by Kulik and Shekhter [16] in 1975.

1.3 Three terminal charging effect devices

The simplest three terminal device based on the charging effect is the single electron transistor (SET) [21], sketched in fig. 1.4. It consists of two ultrasmall junctions in series, isolating an island from the rest of the circuit. The island is capacitively coupled to a gate electrode.

The electrodes and/or the island can be superconducting. In this case, the charge carriers are Cooper pairs (unless $\Delta \ll E_C$), as well as electrons, and one speaks of a ‘superconducting SET’ or S-SET rather than using the term ‘charge-effect transistor’ (CHET) [30].

The charge of the island is the sum of the charge induced by the gate voltage

$$Q_g = CV_g, \quad (1.9)$$

and the number of electrons n in excess of the number of positive charges (protons) in the island. Q_g is a continuous variable, and the charging energy E_{ch} is a function of Q_g and n . For a derivation of the I - V characteristics, see e. g. the review article by Schön [31]. Here we will only state that the ideal SET

- has a Coulomb blockade whose maximum thresholds are determined by the junction capacitances, and
- whose extension is periodic in the gate voltage, with one period corresponding to one elementary charge induced on the gate capacitance.

Ideal means among others that the junctions should be identical; otherwise, the IVC will show a periodic structure known as the Coulomb staircase [16].

1.4 The need for smaller resistors

To understand why (physically) very small resistors with high resistance are desirable for use in single electronics, we shall take a brief look at the influence of the electromagnetic environment on tunnelling in ultrasmall junctions.

1.4.1 Coulomb blockade and electromagnetic environment

Soon after the first single electron devices had been made it was realised that the electromagnetic environment had a profound influence on their properties [32, 33, 34, 35]. The Coulomb blockade in single junction is largely shunted out by the effect of stray capacitances of the leads. Essentially, these lead capacitances make the junction voltage biased rather than current biased. The first observations of the Coulomb blockade were therefore made in systems of two tunnel junctions connected in series (see 1.2.1, where a particular junction was shielded from the environment by another junction with resistance higher than the quantum resistance R_K).

The effect of the electromagnetic environment on ultrasmall tunnel junctions can be calculated using different approaches. One such approach is the theory known as the ‘ $P(E)$ theory’, because it involves a probability density function $P(E)$ describing the emission or absorption of energy during a tunnelling process due to the coupling to the environment [36, 31]. The circuit with the junction(s) and the environment, represented by an impedance $Z(\omega)$, is modelled as an ensemble of harmonic oscillators. The approach follows the model for dissipative quantum mechanics developed by Caldeira and Leggett [37].

A simple alternative model is the horizon picture [38, 39], in which the electromagnetic environment is treated as purely capacitive, and its spacial extension as given by the speed of light and the time corresponding to the energy eV via a time-energy uncertainty relation. Experiments showed [33] that it is this time rather than the traversal time [40] that determines the horizon. The horizon picture has been found to give reasonable results for single and double junction circuits in the normalconducting state [41, 42].

In any case, the Coulomb blockade of single junctions is much sharper if the junction is placed in an environment with high impedance $Z(\omega)$ than in a low-impedance environment. This has been found experimentally [43], and is rather well understood theoretically [31]. Cleland et al. argued that the environment’s impedance can be maximised by contacting the junction with a high-resistivity material with as small as possible cross section [43]. The impedance of the leads should exceed the quantum resistance R_K if the Coulomb blockade is not to be suppressed.

1.4.2 Resistors in single electronics

The fabrication of such high-resistance low-stray capacitance resistors is non-trivial. Cleland and coworkers made thin film resistors of NiCr [43] and achieved a ‘performance’ of $30 \text{ k}\Omega/\mu\text{m}$. This allowed them to observe that the Coulomb blockade was much sharper than with leads of $2 \text{ k}\Omega/\mu\text{m}$.

A series of experiments involving thin film resistors and a single junction was made by Haviland and Kuzmin in 1991 ff. and led to the observation of the Coulomb blockade of Cooper pair tunnelling in ultrasmall Josephson junctions and the Bloch oscillations due to the time correlation caused by the blockade [44, 45, 46, 47, 48].

In all these experiments, the thin film resistors were made from a different material than the junction electrodes or barriers. This introduced the need for a third angle evaporation (using a suspended mask technique), resulting in either a lot of unwanted material or demanding a complicated tear-off process. In addition, such thin film resistors have the disadvantage of not being tunable to a desired resistance value.

The motivation for the experiments described in this report was to develop a fabrication process for resistors that were tunable and made from the same material one would possibly use as electrode material, namely niobium. In general, materials with a high sheet resistance are not easily produced reproducibly. Wong and Ingram [49] have reported a germanium-copper alloy for application in thin film resistors. Still, the difficulty of integrating this material into the single electronics circuit remains.

Two advantages we expect from resistors made by niobium anodisation are due to the oxide encapsulating the structure. First, the oxide should protect it against corrosive influence from the atmosphere, and e.g. from chemicals in lithographic processing steps. We found that indeed our samples, once they ‘survived’ the fabrication process, were quite stable (with the exception of some of the samples in single electron transistor-like geometry considered in 3.3).

The second expected advantage, which we have not yet verified, is that the high volume of the resistors should diminish hot electron effects [50]. These effects are caused by the weakness of the electron-phonon coupling at low temperatures; the passage time of the electrons is too short for them to acquire thermal equilibrium with the lattice (phonons). Another strategy to improve cooling and thus reduce hot electron effects is to increase the volume of the resistor without decreasing its resistance too much by adding cooling fins [50].

An alternative method for making biasing resistors for single electron devices is the fabrication of arrays of relatively large junctions [42, 51]. The integration is straightforward since these resistors are made in the same angular evaporation process as the active element(s). The problem of tuning the resistance is not so serious and mostly a matter of having the right geometric dimensions since the resistance is determined by the oxide thickness, and that parameter is critical for the active elements anyway. As a consequence, for applications not demanding extreme performance, in terms of resistance per capacitance, junction arrays resistors are a viable technology.

1.5 Superconductor-insulator transition in thin films

While the entry into the superconducting state below a critical temperature T_c is a thermodynamic phase transition, the superconductor-insulator transition (S-IT) we will consider in this section is (or ‘may be interpreted as’) an example of a quantum phase transition (QPT) [52]. QPT take (in principle) place at zero temperature, and the S-I phase boundary is crossed by varying a parameter other than the temperature in the system’s Hamiltonian. This can be the charging energy in a Josephson-junction array [53, 54] or the amount of disorder in a metal undergoing a metal-insulator transition (M-IT). Superconducting thin films have similarities with both disordered metallic films and arrays of Josephson junctions [55]. The small grain size generally means that even charging effects are important in these films.

Experimental studies have been performed on quench condensed films, that are films deposited from the vapour phase onto a very cold surface. This technique allows to grow amorphous or nanocrystalline films. Experimental studies on a variety of materials show that the parameter governing the behaviour seems to be the sheet resistance of the thin films. White et al. [56] have measured the superconducting gap with tunnelling experiments and found that the broadening of the gap edges became comparable to the gap itself, and hence superconductivity disappeared, when the sheet resistance at high temperature reached $(10 \dots 20) \text{ k}\Omega/\square$.

Jaeger [57] found that gallium films became globally superconducting when the sheet resistance was below about $6 \text{ k}\Omega/\square$. Experiments [58, 59] suggest that the threshold for the superconductor-insulator transition is a sheet resistance of one-fourth the Klitzing resistance, the so-called quantum resistance for pairs

$$R_Q = \frac{h}{(2e)^2} = \frac{R_K}{4} \approx 6.45 \text{ k}\Omega. \quad (1.10)$$

There is no conclusive agreement to date on whether this value is a universal sheet resistance for the S-IT [60].

In all these experiments, the sheet resistance depended very sensitively on the film thickness; in most cases, a difference of one nominal monolayer can change the sheet resistance over the entire range of the S-IT [55]. This problem was addressed by Wu and Adams [61], who used the same technique we used for the experiments described in this report: the films (Al in his case, Nb in our experiments) were deposited with a certain (relatively high) thickness and then thinned by controlled anodic oxidation.

1.6 Anodisation of niobium

Anodic oxidation or ‘anodisation’ is the process of forming an oxide layer by electrolysis on a metal anode in a suitable electrolyte. Historically, the first major use of anodic oxide films was as dielectrics in electrolytic capacitors [62, 63],

and a lot of development work especially with regard to electrolytes was carried out by industry and is hence scarcely documented in the scientific literature. A general reference on anodic oxide films is Young's 1961 book [64], and niobium is covered in detail in d'Alkaine's 1993 series of papers [65, 66, 67]. Halbritter [68, 69] treats the subject of niobium and its oxides with focus on the interfacial structure. After giving some information on the electrochemistry of niobium and its oxides, we will take a look at various applications of anodisation for micro- and nanofabrication of niobium that are documented in literature.

1.6.1 Electrochemistry of niobium and its oxides

Niobium was discovered by Charles Hatchett in the year 1801 and originally named Columbium. In the following years, it became confused with Tantalum, discovered 1802, with which it occurs mostly in nature, and was finally isolated and rediscovered in 1844 by Rose and named Niobium (after Niobe, the daughter of Tantalos). Both names were used until element 41 was officially named Niobium by IUPAC in 1950, but the name Columbium is to date still used occasionally by the American metallurgical community and e.g. the United States Geological Survey. In metallic form, niobium was isolated for the first time by v. Bolton in 1905.

Early work on niobium anodisation was inspired by potential applications in electrolytic capacitors [63, 70], but Nb electrolytic capacitors did not become a large scale commercial product like those based on Ta. Today, niobium oxides are often studied because they form the surface of superconducting accelerator cavities, and since acceleration is a high frequency application, the surface is very important to the cavity quality. Such cavities used to be made of sheet niobium, but are nowadays also produced from copper covered with sputter deposited niobium [71].

There exist three stable oxides, niobium pentoxide Nb_2O_5 , niobium dioxide NbO_2 , and niobium monoxide NbO , and the solution of oxygen [72] in niobium notated as $\text{Nb}(\text{O})$, with up to one weight percent of oxygen at high temperatures. Niobium pentoxide occurs as NbO_x with $x \in [2.4 \dots 2.5]$, the dioxide and pentoxide only in narrower stoichiometry [73]. Nb_2O_5 is the principal constituent of anodic oxide films on niobium [74, 75]. Its density in bulk amorphous form is $\varrho = 4360 \text{ kg/m}^3$, and its dielectric constant $\varepsilon \approx 41$ [75]; values for thin films might deviate from this value, though. Nb_2O_5 is an insulator, NbO a superconductor with $T_c \approx 1.4 \text{ K}$.

The microstructure of an anodic oxide film on niobium is rather complicated. The outermost layer is Nb_2O_5 , followed by a thin layer of NbO_2 followed in turn by NbO . This sequence was determined by Gray et al. using ion scattering spectroscopy [73]. It is noteworthy that they found a more gradual falloff in stoichiometric oxygen content from Nb_2O_5 to Nb on anodised foils than in natural oxide layers. Halbritter points out that the interface between niobium and its oxides is not even but serrated [76]. This serration is stronger for 'bad' niobium as measured by the residual resistance ratio (RRR), the ratio of resistivities at room temperature and at 4.2 K or just above the transition. Niobium

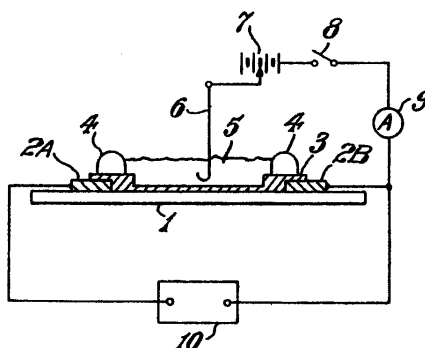


Figure 1.5: Anodisation setup for resistor fabrication, reproduced from Western Electric Company's 1959/1960 patent specification [79]. (3) is a metal strip, (10) a resistance monitoring device.

deposited by thermal evaporation is, compared to sputter deposited material, always 'bad', but evaporation in conjunction with a liftoff mask offers more flexible patterning techniques.

The reason for the serration of the interface is the volume expansion from Nb to Nb_2O_5 by a factor of about 3 [77] in combination with the mechanical properties of the compounds involved. Nb (density $\rho = 8570 \text{ kg/m}^3$ at room temperature) is relatively soft, and niobium pentoxide microcrystallites cut into the metal. This serration does not occur on the metals NbN and NbC that are harder than Nb; carbon inclusion in the interface is known to improve the quality of Nb based tunnel junctions [78].

1.6.2 Micro- and nanofabrication by anodisation

For purposes of micro- and nanofabrication, anodic oxidation is basically used as a means to remove Nb metal; since the oxide is not removable without affecting the underlying metal, it often becomes an integral part of the design as an insulating layer.

Anodisation thinning of Nb metal strips (or other anodisable metals) for the fabrication of tunable thin film resistors was patented to Western Electric Company in 1959/1960 [79]. Figure 1.5 is a reproduction of a drawing from their patent application, showing a setup quite similar to that used by us for microanodisation described below (2.3, cf. figure 2.8). A metal strip (3), deposited on a substrate (1), is covered with electrolyte (5) confined by a mask structure (4). The resistance of the samples is monitored via two leads (2) by some means (10), and the anodisation voltage between the metal strip and the cathode (5) is adjustable (7,8), e.g. such that the anodisation current (9) is kept constant. The latter does not apply in our case; we will come back to the anodisation process for resistor fabrication in detail in 2.3.1 and 2.3.2.

In large scale, anodisation is used for the production of small junctions from prefabricated three layer sandwiches ($\text{Nb}/\text{AlO}_x/\text{Nb}$) through the selective niobium anodisation process (SNAP [77]). The top layer metal is oxidised where a photolithographically defined resist mask exposes it to the electrolyte, and then suitable contacts are made to the bottom layer and the unoxidised part of the top layer. This technique allows making high quality junctions since the trilayer can be formed under conditions and by methods (e.g. sputtering) that cannot be used for deposition through a liftoff mask. Anodisation voltages are usually monitored to determine the etch end.

Ohta et al. used anodisation to thin a weak link [80] and observed a transition to a tunnel Josephson junction in the temperature dependence of the critical current, and Goto made variable thickness bridges (VTB [81, 82]) in Nb strips several micrometres wide by anodising through a mask with an opening of only 200 nm, produced from silicon monoxide by shadow evaporation at a resist mask step. Here also a transition to Josephson junction behaviour was found, this time manifesting itself in the occurrence of Shapiro steps under microwave irradiation. Both Ohta and Goto anodised without a monitoring device and assumed a certain Nb consumption proportional to the applied voltage, an assumption whose validity we shall inspect in 2.3.2.

Anodisation fabrication and single electronics were combined when Nakamura et al. made the so-called anodisation controlled miniaturisation enhancement (ACME [83]) of single electron transistors in 1996. They made single electron transistors in the ‘conventional’ aluminium technique with shadow evaporation and oxidation [84, 85] and subsequently anodised the complete structure in order to minimise the junction area, thus the capacitance, and raise the operating temperature. In such a sample, they were able to observe a modulation of the source-drain current with gate voltage up to temperatures of 30 K. During the fabrication, they monitored the resistance through the SET continuously, and were able to increase its value by two orders of magnitude. Preexisting asymmetries of the junctions in the SET seem to be enhanced by this process, so that most of the samples showed a Coulomb staircase.

Chapter 2

Nanofabrication and microanodisation

In this chapter, the techniques used for the nanofabrication and microanodisation of niobium samples will be described. Figure 2.1 gives an overview over the fabrication process. Some of the information is of special interest with regard to the equipment used, namely the JEOL JBX 5D-II electron beam lithography system; most of the specific details, though, may be found in the recipe appendix C.

2.1 Substrate and carrier system

Substrate material for all our samples are silicon wafers in (100) orientation with a diameter of two inches and a thickness of about 0.25 mm that have been thermally oxidised to an oxide thickness of about 1 μm . Since doping and resistivity of the silicon do not play a role, wafers in sufficient quality can be obtained at a price of less than 10 ECU each. A disadvantage of oxidised silicon (compared to unoxidised silicon) as a substrate material for single electronics is that it makes components more prone to damage from static electric discharges. On the other hand, it allows testing of components at room temperature, saves time and chemicals otherwise needed to remove the native oxide, and enables anodic oxidation of materials deposited on the substrate without having to worry about the anodisability of the silicon itself.

Standard chip size for our measurement equipment is $7 \times 7 \text{ mm}^2$, limited by the space available in the commercial dilution refrigerator (see 3.1.1). Cabling in this refrigerator limits the number of contacts to sixteen, of which thirteen are dc leads and three coaxial cables for rf signals. Contact between the leads and the chip is made by spring-loaded probes ('pogo-pins').

The centre of each chip contains an area of $160 \times 160 \mu\text{m}^2$ where nanopatterns are defined by electron beam lithography. From this area, dimensioned to equal four 'fields' of the EBL system in highest resolution mode (see glos-

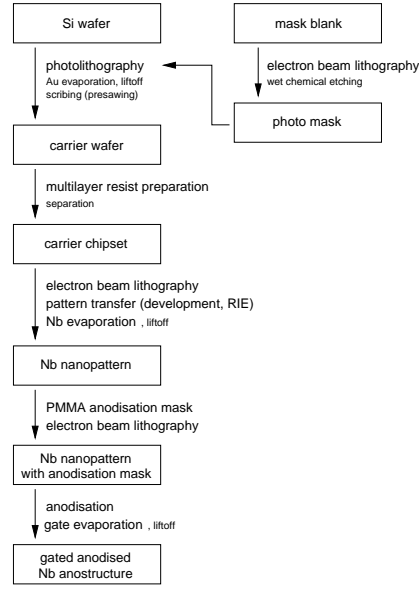


Figure 2.1: Fabrication of anodised Nb nanostructures with gates: process step flow scheme.

sary appendix B for definitions), gold leads connect to the contact pads for the pogo-pins situated about two and a half millimetres away from the chip centre (a certain minimum distance is advantageous for the subsequent anodisation step, to facilitate placing of a droplet of electrolyte).

Besides the contact pads and leads, the gold chip pattern comprises a chip number field, visible with the naked eye and used to orientate the chip during handling, and four alignment marks ('wafer marks', see glossary). This pattern is most economically created by photolithography.

A process for carrier chip photolithography [86, appendix to chapter 4] had to be abandoned to comply with environmental regulations restricting the use of toxic and carcinogenic chemicals. Instead, a new process was developed that not only eliminates chlorobenzene but also requires less baking and chemical treatment steps. A detailed account of this process is given in C.2. High quality in the photolithography is especially important for the alignment marks, since several alignments are performed during the whole fabrication process.

After photolithography, the wafers are presawed ('scribed') along the chip edges from the back side and separated into sets of chips for further handling; generally a set of two by two chips is processed at a time.

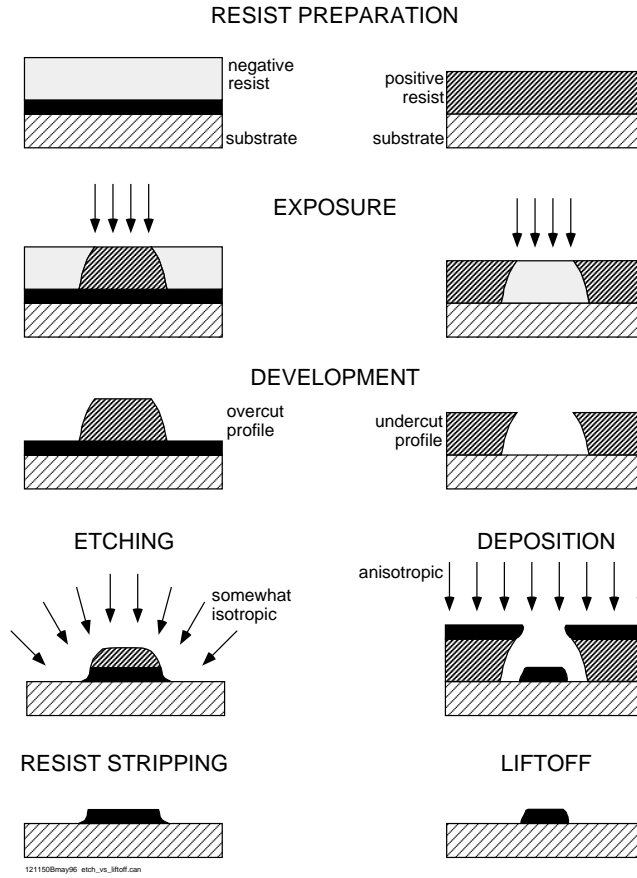


Figure 2.2: Basic pattern transfer types relevant for nanofabrication: etching and liftoff processes. Note the widening of the exposure profile due to scattering of the electron beam, the resulting overcut profile in negative and undercut profile in positive resist. Isotropy of etching and mask erosion lead to a concave, clogging of the liftoff mask on the other hand to a convex profile of the patterned material in the respective processes.

2.2 A niobium liftoff nanofabrication process

There are two basic pattern transfer process types relevant for nanofabrication, namely etch processes and liftoff processes. Figure 2.2 shows a comparison of these two. In the case of an etch process, the material that is to be patterned is deposited on the whole substrate, covered with resist and etched away where the resist has been removed after exposure and development. In a liftoff process, the resist is patterned first, and the relevant material deposited onto the patterned resist. It is removed ('lifted off') together with the resist mask in a strong

solvent.

A special form of liftoff process is the angular evaporation technique [84, 85].

Making weak links in very thin niobium films by an etch process is very difficult since native oxides cause a significant uncertainty in the initial etch rate. Since the angular evaporation technique was assessed essential for our samples in SET-like geometry (and promises the possibility to make overlap junctions), we decided to build know-how in a niobium liftoff nanofabrication process suitable for the angular evaporation technique.

2.2.1 Pattern design and compilation

Since the JEOL JBX 5DII system is a vector scan system with a scan step of only 2.5 nm in highest resolution mode, patterns can be designed as vector drawings without regard to future pixellation. All patterns used for this work were designed using the AutoCAD programme on a Digital VAX workstation. They were exported as Drawing Exchange Format (DXF) drawings and converted to JEOL01 code [87] by a local programme and then via a sequence of conversion steps to JEOL's scanner format used for the control of the EBL system.

Parallel to the drawing, information on pattern placement and exposure doses is supplied in form of the so-called jobdeck and schedule files (see glossary appendix B).

By the time of this writing (April 1997), the JEOL01 format has been largely obsoleted by the introduction of the PROXECCO proximity correction programme [88] (see 2.2.3), which produces output in the industry standard Calma stream format (GDS II)[89].

2.2.2 Four layer resist system

The melting point of niobium is 2468 °C, so that it can only be thermally evaporated by electron gun heating and not from boats. Liftoff masks are thus subjected to intense thermal load, and all-polymer masks are generally regarded as unsatisfactory for Nb patterning. Even the system of a germanium mask supported by PMMA or P(MMA-MAA) used for the fabrication of ultrasmall tunnel junctions [90] is easily damaged.

A more suitable system is an aluminium mask on a polyimide support used by Jain et al. [91]. Liftoff is difficult, however, since polyimide is quite resistant to strong solvents like acetone. Harada addressed this problem by introducing the four layer resist [92] whose structure can be seen in the top left panel of figure 2.3: a germanium mask supported by a layer of hard-baked photoresist S-1813 end equipped with a PMMA bottom layer to enable liftoff. Like in many resist systems for submicrometre lithography, the top layer patterned by EBL consists of PMMA.

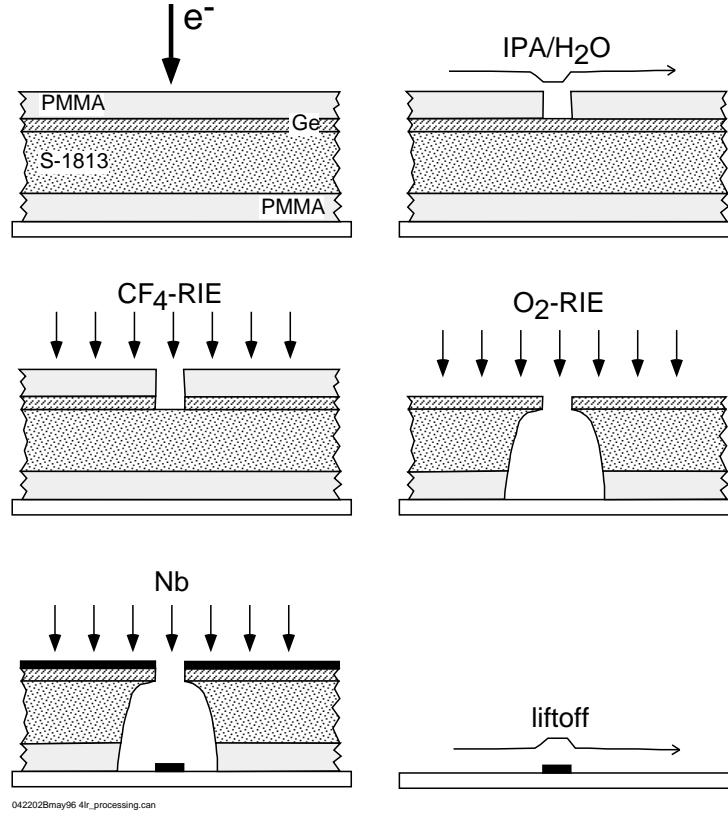


Figure 2.3: Four layer resist: overview of processing steps for Nb liftoff nanopatterning. After exposure and development of the top layer, the pattern is transferred to the germanium mask by reactive ion etching with carbon tetrafluoride. Subsequent RIE with oxygen creates the undercut profile needed for a liftoff mask.

2.2.3 Pattern definition with electron beam lithography

Electron beam lithography is a pattern generation technique based on physicochemical modification of matter under electron beam irradiation. In its most usual form, an organic substance (‘resist’) either increases or decreases in solubility in a proper agent (‘developer’) under the influence of the e-beam. Resists are called positive in the first and negative in the latter case. A certain dose is required to achieve the modification, defining the sensitivity of the resist. The ratio of the solution rates of exposed and unexposed resist is called the contrast of the resist under certain process conditions. PMMA is a positive resist with a rather low sensitivity, but with good contrast.

An electron beam lithography machine generates a pattern by sweeping a

very fine beam over the sample, using magnetic lenses, and blanking the beam where exposure is not desired. Much of the technology involved stems from scanning electron microscopy, and the cheapest EBL machines are indeed SEMs with some extensions. Our JEOL system, however, is a commercial machine designed for high precision lithography on large areas, which was very useful for the quantum dot work described in the appendix omitted from this WWW edition. All patterns were written in the highest resolution mode (for insiders: first aperture, fifth lens). The lowest current, giving the smallest beam diameter, was 20 pA, and the maximum current used, one that could be achieved reliably even with an aged emitter, was 1 nA. These two currents were used for lithography of the fine patterns and coarse leads, respectively. Division of patterns into low and high current patterns requires some additional adjustment time, but can give substantial savings in exposure times, thus allowing for numerous test patterns. Such test patterns with varied dose are valuable tools for the assessment of development process steps.

Finding the right dose for a pattern is a nontrivial problem due to the proximity effect. Forward scattered, backscattered, and secondary electrons place an electron dose outside the area directly hit by the electron beam. For large beam diameters, even the nonuniform current density in the beam (assumed to be a Gaussian) must be taken into account. As a consequence of the proximity effect, large areas consisting of many pixels require a lower averaged irradiation dose because surrounding pixels contribute to the dose in a certain spot. Conversely, small patterns need to be exposed with a higher dose in order to develop properly. There are in principle three ways of performing the proximity correction, i. e. the assignment of different doses to pattern details of different width and in different surroundings:

1. Trial-and-error: based on some initial guess, test exposures are performed and the results assessed by electron microscope inspection.
2. Rules-of-thumb: proximity correction can be estimated using e.g. the formulas given in [93, appendix C].
3. Correction programmes: a number of commercial software products for proximity correction are available that calculate local correction factors from CAD data and a suitable correction function. Such a correction function, in turn, is generated by simulation programmes, usually using a Monte Carlo approach.

Most of the patterns described here were designed using manual proximity correction with the trial-and-error method, leading to the doses given in C.4. Recently (March 1997), however, the transition to PROXECCO-corrected patterns has been initiated. Simulations are performed using a local programme aptly named `mcarlo`. Relevant parameters are given in C.5.

2.2.4 Pattern transfer

A simple developer for PMMA is a mixture of isopropanol and water. As soon as possible after exposure, the patterns were developed using the concentration, times etc. given in C.6.

Pattern transfer to the metal mask

The openings in the EBL-patterned PMMA top layer were transferred to the germanium layer by reactive ion etching (RIE). RIE is a combination of chemical etching and physical sputtering. The sample is placed inside a low pressure reaction chamber on an insulated electrode, and a reactive gas ('process gas') is let into the reaction chamber. A radio frequency cold plasma discharge is then ignited in the chamber. The process gas becomes partially cracked by the discharge, creating highly reactive radicals that can reach the sample because their mean free path is long enough in the low pressure. These radicals provide the chemical etching, which is essentially isotropic. Additionally, molecules accelerated in the electric field have a sputtering effect. The lower the chamber pressure, the higher is the anisotropy of this sputtering. Near the electrode on which the sample is placed, a dc bias voltage occurs between the electrode and the plasma potential due to different mobilities of positive and negative ions. The anisotropy of the etching increases with this dc bias.

A suitable reactive gas for germanium etching is carbon tetrafluoride CF_4 . Our RIE system was not equipped with an etch end detection, so that the required etching time had to be estimated based on experience, allowing some extra margin since reactive ion etching processes tend to be somewhat irreproducible. Etch rates may vary depending on contaminations present in the chamber, or on the size of the sample areas, just to name a few factors. Overdoing this etch step resulted in a slight increase in linewidths, but this increase was considered tolerable.

Successful etching of the germanium layer is clearly visible by optical microscope inspection. While developed PMMA areas appear just slightly brighter than their surroundings in an optical microscope, the etched Ge areas are much darker.

Etching of the support layers

Both the hardbaked photoresist and the PMMA bottom layers were etched with RIE using oxygen as reactive gas. A higher pressure than in the Ge etch step was used to increase the anisotropy of the etch rate to create the desired undercut profile. Another advantage of higher pressure is that the physical sputtering, leading to damage of the suspended Ge mask parts, is reduced.

Other than in the Ge etch step, the lack of an etch end detection is rather unfavourable here, because unnecessarily long etching causes damage of the Ge mask that could otherwise have been avoided. Figure 2.4 is a scanning electron micrograph of an etched four layer resist mask. The undercut is clearly visible if one uses acceleration voltages of (5...8) kV. The suspended bridge in this picture

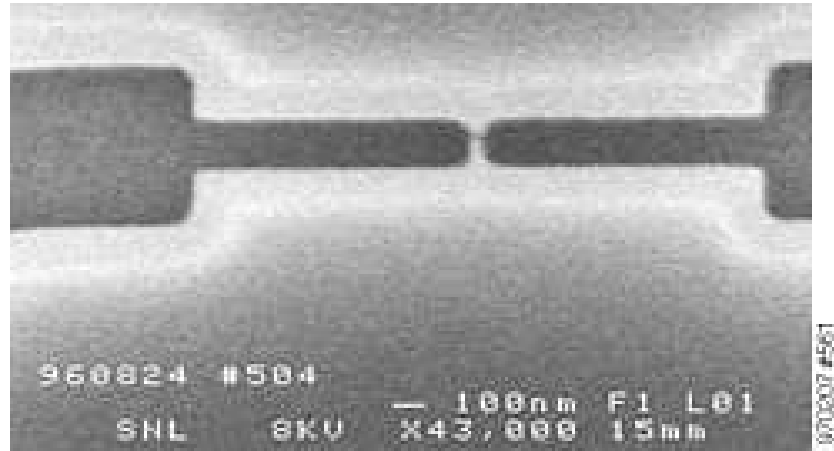


Figure 2.4: Four layer resist mask after pattern transfer and reactive ion etching steps. The darkest regions are the substrate (oxidised silicon), adjacent light areas show the undercut created in the oxygen etching step. The bridge in the center is damaged by a tiny crack.

is damaged in the form of a tiny crack. More careful timing of the oxygen etch step and use of Teflon pedestals to adjust the position of the sample in the reaction chamber can reduce the risk of such damage.

Surface quality and contamination

The major problem associated with pattern transfer entirely by plasma etching is that of surface contamination. Figure 2.5 shows an example of grainy surface contamination that is frequently observed on our samples, and is reported (at least unofficially) by other users of RIE-only pattern transfer. The exact origin of this contamination is unknown. Gentler etching seems to reduce this contamination, and corroborates the assumption that it is caused by the redeposition of sputtered material during the oxygen etch step. Since the contamination occurs mostly in wide open areas and hardly affected line shaped structures below 200 nm width, it could be tolerated for our purposes.

Recently (March 1997), a mask based on a polyimide bottom layer was introduced at the Swedish Nanometre Laboratory. The final pattern transfer step here is a wet chemical development, and this process might be an alternative to the four layer process described above.

Angular evaporation of niobium

The evaporation of good niobium requires large power and ultra high vacuum (UHV). The first requirement is due to the high melting point and can be met with the use of electron gun heating. The latter requirement, however, is

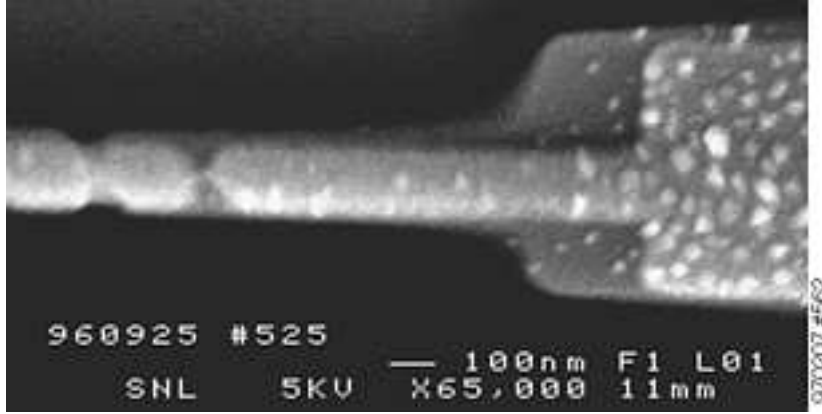


Figure 2.5: Grainy contamination occasionally observed on large Nb areas (right).

harder to meet since under the immense heat during evaporation, most UHV systems suffer from outgasing. For the samples described in this report, a non-bakable multipurpose HV system was used, not a UHV system, and reasonably low pressure had to be achieved by a series of preevaporations and long-time pumping. Still, the pressure during evaporation was typically about $(3 \pm 1) \cdot 10^{-5}$ Pa, which gives pretty poor niobium with a T_c of the order of 1.5 K. A new evaporation system tailored to the specific needs of niobium evaporation is presently under test and gave films with a T_c around 9 K in 100 nm thick films.

The film thickness was monitored during evaporation with a conventional, water-cooled crystal resonance bridge, and controlled ex situ with an Alphastep stylus-method profilometer. For a typical film thickness of 20 nm, the accuracy of the thickness control appears to be not better than 10 %, which is a rather strong limitation for the fabrication of double weak link structures depending on the symmetry of the two weak links. Figure 2.6 is a schematic drawing of the angular evaporation process we used for the fabrication of samples with two weak links in SET-like geometry. In this approach, the length $l_1 \approx l_2$ of the weak links is defined by lithography (as the width of a suspended bridge), while the island length l_c is created by an overlap and can in principle be made very small. Subsequent anodisation (bottom panel) creates an oxide layer with thickness d_a , thinning the weak links to an averaged thickness d_r . In this sketch, we have neglected the deposition of material on the suspended bridge, leading to an asymmetry in the shape of both weak links, and the swelling of the film during anodisation.

A scanning electron micrograph of such a double weak link structure, consisting of two 20 nm thin spots in an otherwise 40 nm thick film, is given in figure 2.7. This sample was made by evaporating the niobium under angles of $\pm 22^\circ$ to the substrate normal.

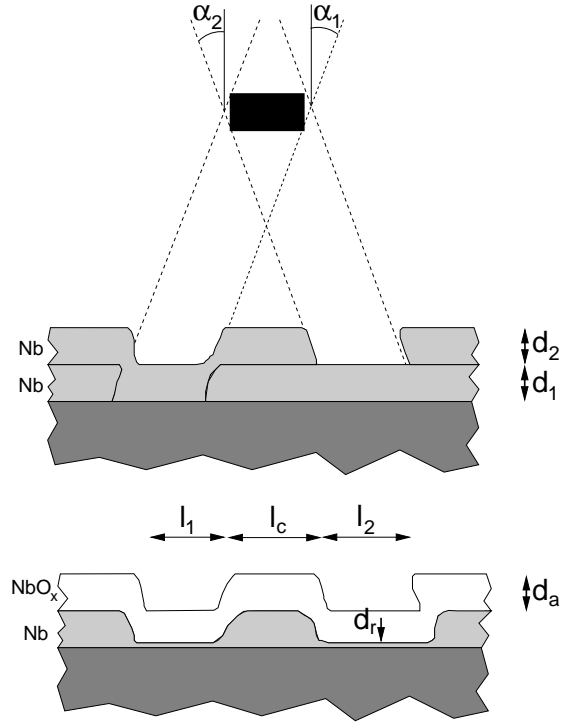


Figure 2.6: Fabrication of samples with two weak links in single electron transistor-like geometry. Angular evaporation with a suspended bridge mask (top) defines the two weak links separated by an island. After anodisation (bottom), the remaining Nb is much thinner in the weak spots. Neglected in this sketch are the deposition of material on the mask and the swelling of the film during anodisation.

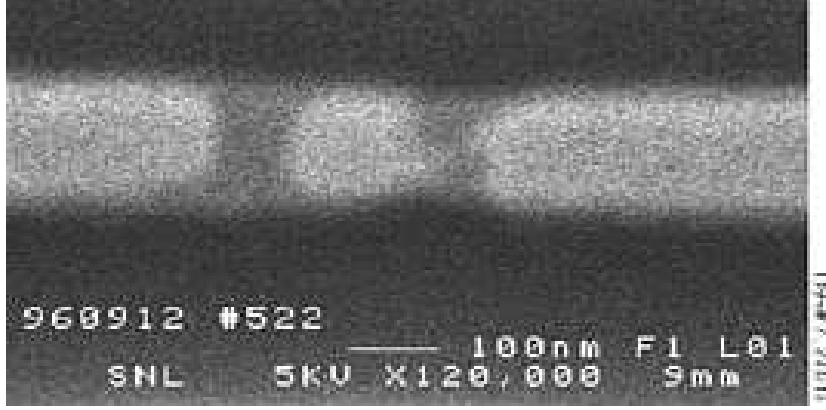


Figure 2.7: Variable thickness weak links in a Nb wire made by double angle evaporation technique, after deposition and before further processing.

2.3 Microanodisation of niobium

In the following section, we will first introduce the equipment and processes used for anodisation, and then present results on anodisation dynamics that are of direct importance to our goal of fabricating tuned resistors and weak link structures. We shall especially take a closer look at oxide growth under constant voltage bias.

2.3.1 Experimental setup and procedures

Figure 2.8 shows a schematic drawing of our setup for niobium microanodisation. In comparison with the historic drawing (see figure 1.5), the important differences are a microfabricated anodisation mask, a cathode integrated on the chip, and a specified means of resistance monitoring.

Anodisation mask design and preparation

The anodisation mask consists of a simple PMMA layer, at least $1.5\mu\text{m}$ thick. It meets the requirements for stability against dielectric breakthrough under the required cell voltages (of up to almost 30 V), can relatively easily be applied and patterned, and removed. It can even be used as liftoff mask for gate electrodes, because a slight undercut profile is created in such thick resists by backscattered electrons.

An optical micrograph of an anodisation mask, here over a long resistor wire sample, is given in figure 2.9. The photo shows the window over the wire, to the right, and another window over a gold contact lead on the left. This gold lead served as cathode. Since the amount of chemicals involved is small even in relation to the size of the electrolyte drop, chemical processes at the cathode

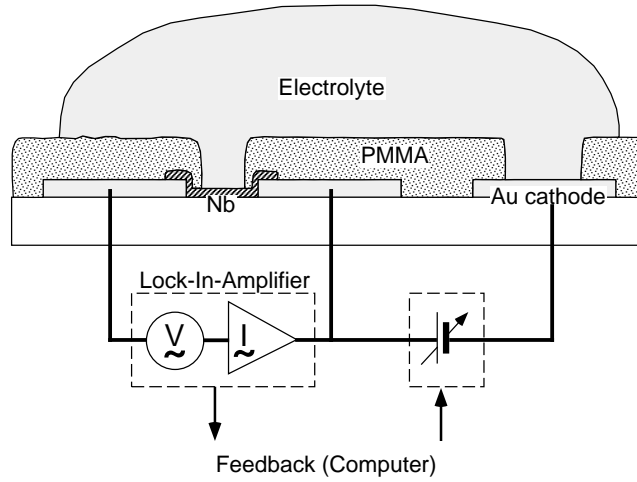


Figure 2.8: Experimental setup for microanodisation of niobium nanostrips (schematic). In reality, electrical contacts are placed at the chip perimeter, well away from the electrolyte droplet.

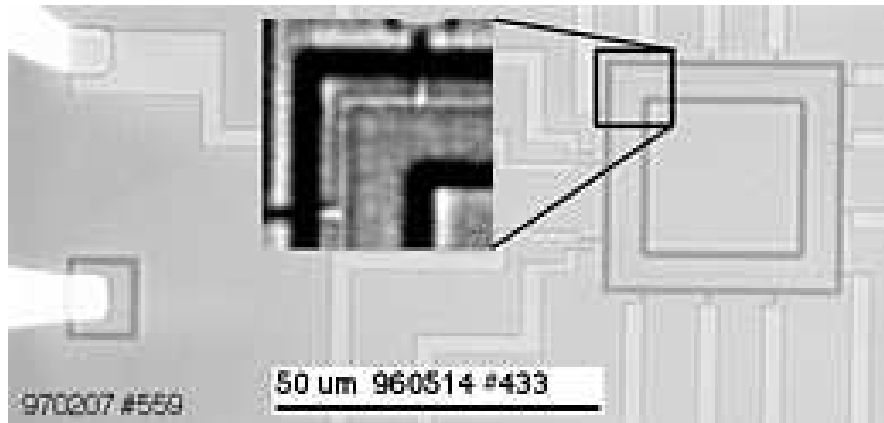


Figure 2.9: Anodisation mask, optical photograph. Light structures on the left side are gold contact fingers, the lower one being used as on-chip-cathode. The square frame shaped window on the right exposes the Nb wire, visible as a thin white line with two leads in the detail magnification.

have no major importance, and the cathode can be made of practically any metal that does not form an insulating surface oxide; niobium does not work well. The integrated cathode very close to the chip centre means that only a tiny drop of electrolyte is needed, in practice the smallest drop one can create with a syringe and place by hand. The need of inserting a cathode into the electrolyte is eliminated, and the chip can be moved in the sample holder with the electrolyte in place, which is a great advantage.

Electrolyte

As mentioned before, a lot of the development of suitable electrolytes has been done in industry many decades ago and is poorly documented in the scientific literature. Many recipes are based on experience rather than a deep understanding of the process details. Demands for a good electrolyte are stability and a low vapour pressure. In the case of an electrolytic capacitor, this reduces the need for hermetically sealed encapsulation, and it is a very welcome property for us, since a change in composition during the anodisation due to exposure to atmosphere is undesirable.

A very important property of an electrolyte for anodic oxidation is that it should be incorporated as little as possible into the oxide film. More precisely, instead of anodic oxide film (AOF) one speaks of anodic film (AF) [94], when the incorporations from the electrolyte are taken into account.

Niobium has the rather pleasant property that it forms a nonporous oxide with many different electrolytes [63], unlike valve metals with incomplete valve action (“unvollständige Ventilwirkung”, [63]) like aluminium. In the latter case, many electrolytes have a solvating effect on the formed oxide, leading to a porous oxide structure. Contamination, especially by halides, is also known to increase the porosity of aluminium AF [94]. For some applications, this is exactly desired, like for the surface treatment of aluminium where pigments are brought into the pores, but for electrolytic capacitors, a strong uniform and thin oxide is essential.

Possible electrolytes for niobium anodisation are saturated boric acid [95] or an aqueous solution of sodium tetraborate and boric acid [96]. We used, however, an aqueous solution of ammonium pentaborate mixed with ethylene glycole. These compounds have been in use since the 1940's, and we could trace back our exact recipe to a 1967 paper by Joynson [97]. Originally used for the forming of pinhole-free oxide films, the same electrolyte was used by Kroger for the selective niobium anodisation process [77]. The electrolyte was designed for use at an elevated temperature of 120°C [97], but works in principle at room temperature, if it is stirred and heated to about 100°C for a few minutes, not more than two days prior to use. After two days, precipitation occurs. For niobium anodisation, the prepared solution could be used for at least one year without any noticeable change in properties. The stability and operability over a large temperature range are typical properties of a good capacitor electrolyte.

Ethylene glycole seems to have several positive effects: it influences oxygen chemisorption and promotes the formation of more stoichiometric oxides [98], and this particular electrolyte is known to show little incorporation of electrolyte

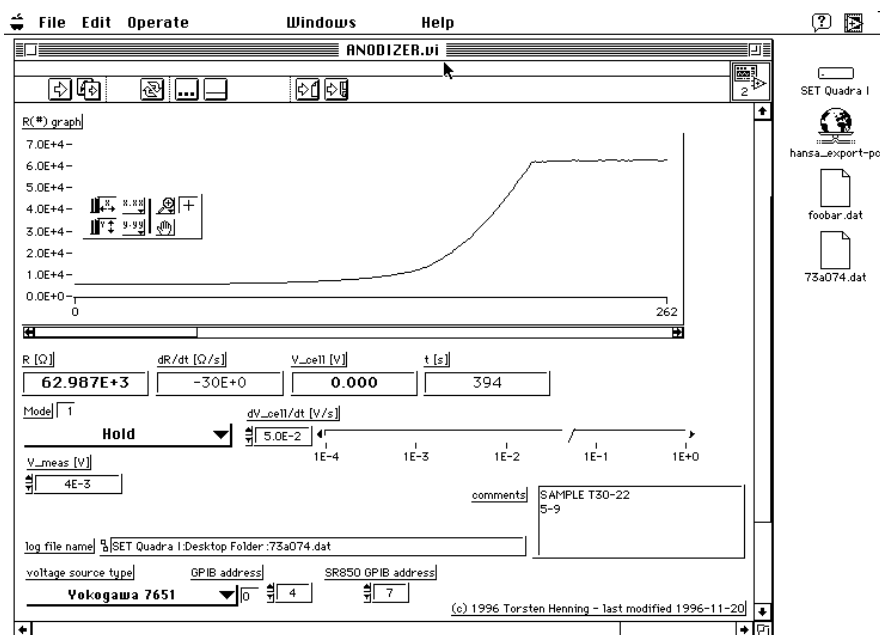


Figure 2.10: Graphical user interface of the resistance monitoring and anodisation voltage control programme. The main display shows the resistance as a function of time.

matter into the anodic film [99]. Side reactions occur at higher voltages [99] and appear negligible for our work, where 30 V is never exceeded.

Resistance measurement and control

The requirements for a resistance monitoring device are: a certain precision, the ability to work in spite of the potential difference between the sample and the electrolyte and cathode, and a negligibly small distortion of the anodisation field to avoid systematic skewing of the anodisation profile. All these requirements are met by using a lock-in amplifier.

We used a Stanford SR850DSP amplifier in current measuring mode, applying a sine shaped excitation with typical rms amplitudes of 4 mV, for very high resistive samples up to 32 mV. With a suitably chosen time constant, resistance measurement accuracies of a few percent can be achieved. Since the cabling of the sample holder was quite open and pickup non-negligible at low frequencies, a measurement frequency of 3000 Hz was used for most of the samples mentioned here.

Careful grounding of the measurement equipment and of the syringe when applying the drop to the chip are strongly recommended.

Resistance and anodisation value readings were taken automatically via a

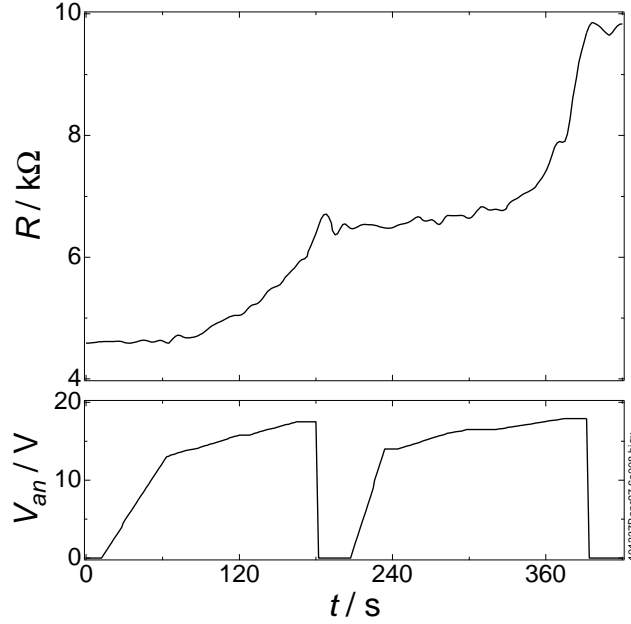


Figure 2.11: Anodisation process. The resistance R along the wire sample increases irreversibly with the anodisation voltage V_{an} and with time.

GPIB equipped Macintosh and logged. A graphical user interface implemented in LabVIEW allowed the operator to monitor the resistance value and adjust the anodisation voltage ramp rate accordingly. Figure 2.10 is a screen dump of this user interface, showing the resistance monitor display and controls for ramp mode and ramp rate and demonstrating the degree of control and smoothness of the resistance tuning.

The sample resistance increases irreversibly with time as the anodisation voltage is applied. The rate of resistance increase in turn is a complicated function of voltage and time itself. In figure 2.11, the time evolution of the resistance and the anodisation voltage for one specific sample are plotted. The resistance values are low since this was a weak link sample, and most of the resistance was contributed by contact resistances in the two probe measurement configuration. In spite of the somewhat noisy data, one can see that the resistance along the sample (top panel) remains constant as the anodisation voltage (bottom) is zeroed.

2.3.2 Anodisation dynamics

As mentioned before, the notion of an ‘anodisation constant’, i.e. a linear dependence between anodisation voltage and the thickness of the metal consumed,

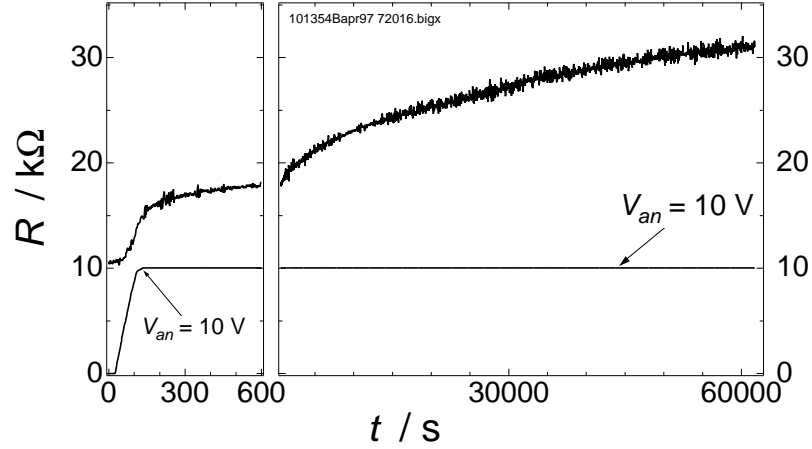


Figure 2.12: Long time anodisation process. As the anodisation voltage is ramped to 10 V (lower trace), the sample resistance rises rapidly in the beginning (left panel). The anodisation voltage is then held constant, and the sample resistance continues to increase over more than sixteen hours, demonstrating that there is no limiting thickness for anodic oxide grown at constant voltage.

does not hold in cases where the current density is not kept constant all the time. Since our anodised areas were so small that the anodisation currents were not accessible to measurement, we only measured the resistance along the sample and fixed (or ramped) the anodisation voltage instead. The nonlinear dependence of oxide growth on voltage and time is well illustrated by figure 2.12. In the process depicted there, the anodisation voltage was ramped up to a fixed value (10 V) in 100 s and then kept constant for more than sixteen hours. All the time, the resistance continued to increase measurably. The rate decreased, but under these conditions, the oxide would theoretically continue to grow until the strip were completely oxidised. This effect can be exploited for the precision tuning of resistors. By stopping the voltage ramping well below the desired resistance value and simply waiting and zeroing the voltage as the desired resistance is reached, one can achieve a resistance tuning whose accuracy is in principle only limited by the measurement accuracy of the resistance monitor.

2.4 Top gate electrodes

The deposition of the overlapping gate electrodes onto the samples in SET-like geometry was the last fabrication step. After some notes on the fabrication itself, we will take a look at the insulation properties of the anodic oxide.

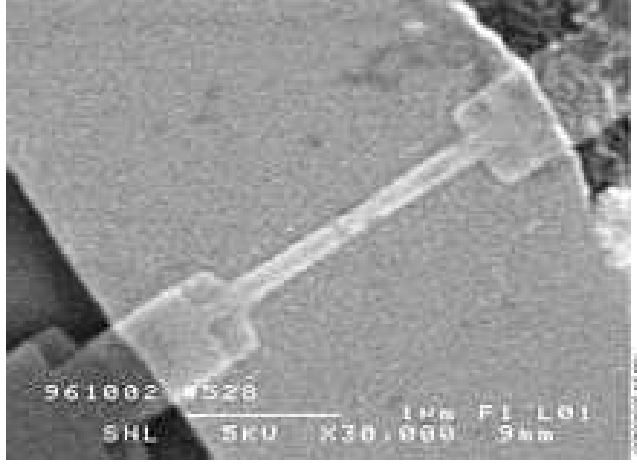


Figure 2.13: Gold top gate on an anodised sample with two weak links (barely visible in the centre), following the contours of the anodisation mask.

2.4.1 Preparation

Making the overlapping gates was quite straightforward. The samples were carefully rinsed with deionised water as soon as possible after the anodisation process. The use of ultrasonic excitation seems to have a negative effect on the anodised samples, most of them were destroyed when such a cleaning process was tried out. A gentle surface ashing with oxygen RIE was found to provide sufficient adhesion of gold to the samples. 50 nm Au were evaporated to ensure continuity over the sample edges. These gates had a two terminal resistance of about 60Ω at a length of $160 \mu\text{m}$ and an initial width of $8 \mu\text{m}$, narrowing down to $3 \mu\text{m}$ over the samples. Figure 2.13 is a scanning electron micrograph of a top gate deposited on a SET-like sample. Contaminations were no major problem, in spite of the fact that the present implementation of the anodisation technique in our laboratory involves no special efforts to eliminate particle contamination.

2.4.2 Electrical properties

The most obvious demand in using a combined anodisation and gate liftoff mask is of course that no metal be deposited on non- (or not sufficiently) anodised areas. This requires a good wetting of the niobium by the electrolyte, and indeed we found no electrical shorts or failures to anodise niobium that had to be attributed to insufficient wetting. The narrowest mask structures were about $3 \mu\text{m}$ wide, and every anodisation window was at least $8 \mu\text{m}$ wide in one direction.

In all but very few samples that we tested at low temperatures, the insulation between the gate electrode and the sample was found to be very good.

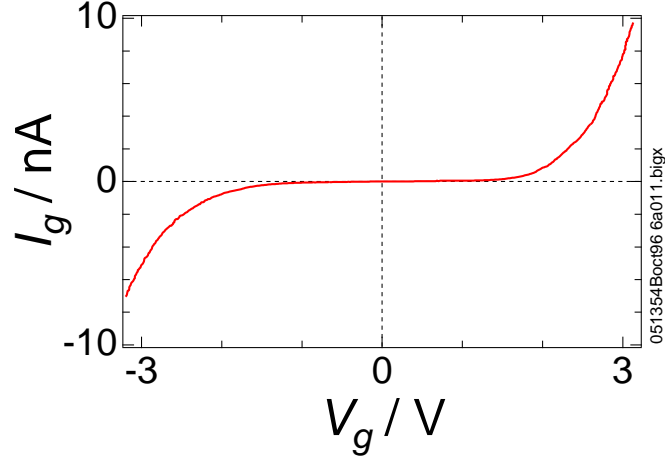


Figure 2.14: Current-voltage characteristic for the leakage current between gate and source-drain of a sample in SET-like geometry.

Figure 2.14 gives an example of a current-voltage characteristic for the leakage current through the gate. Up to gate voltages of about 1.5 V, the gate current was too small to be measured with our equipment, which translates into an insulation resistance of better than 30 G Ω . For higher gate voltages, a measurable current flow set in. For other samples, this point lay at about 0.5 V. In transport measurements through the sample's drain and source, this resulted in a shift of the measured IVC and was easily detected.

Chapter 3

Electronic transport in anodised niobium nanostructures

After introducing the measurement setup common to all experiments, we will present the results of transport measurements on resistor wire samples and on samples with two weak links in single electron transistor-like geometry.

3.1 Measurement setup and procedure

As mentioned in the introduction, measurements on single electron devices may require very low temperatures, and sometimes shielding from the (high frequency) electromagnetic environment. We will briefly take a look at our measurement setup under these aspects.

3.1.1 Cryogenics

The first measurements were performed in a noncommercial dilution refrigerator that reached temperatures down to 95 mK. The temperature could be measured with a resistance thermometer calibrated over the whole accessible temperature range. Most measurements documented in this report were, however, done in a commercial dilution refrigerator of type TLE 200 from Oxford Instruments. A germanium resistance thermometer was calibrated down to 45 mK, and the base temperature of the cryostat was below 20 mK, as estimated from a preliminary measurement with nuclear orientation thermometry. A magnetic field up to 5 Tesla could be applied perpendicular to the sample. With a ramp rate of 0.1 T/min, the sample was warmed to approximately 40 mK by eddy currents.

3.1.2 Shielding and Filtering

The cryostat was placed in a steel enclosure ('shielded room'). Inside this enclosure, all electronics was analogue. Leads into the shielded room were passed through filters in its wall. Inside the cryostat, the leads were multiply filtered. The most prominent part of the filter design are Thermocoax coaxial cables whose excellent filter properties were pointed out by Zorin et al. [100]. More information about the cryostat and the filter design and properties can be found in [101].

3.1.3 Measurement electronics

From the sample, the DC leads went via said Thermocoax filters and multiply thermally anchored wires to an amplifier box on top of the cryostat at room temperature. The bias voltage was symmetrised with respect to ground and fed to the samples via high ohmic resistors in the mentioned amplifier box. Voltage drops over the sample and over the bias resistors (proportional to the current) were picked up by low noise amplifiers, and the amplified voltages sent outside the shielded room for registration. Details about the measurement electronics can be found in Delsing's PhD thesis [93].

Signals were measured with digital voltmeters, initially with DMM of type Tektronix DM5520 with a buffer capacity of 500 points, later with Keithley 2000 DMM storing 1024 data points. The measurement times were synchronised with a Keithley 213 voltage source providing the bias voltage, which was stepped rather than swept continuously. Gate voltages were either generated with a second port on this Keithley 213 source, or with a Stanford Research Systems DS345 signal generator.

Unless explicitly mentioned otherwise, the sweep of the bias or the gate voltage was always bidirectional, starting and ending at one of the edges of the swept voltage region.

All data were registered electronically with the help of a GPIB equipped Macintosh. For historical and practical reasons, the measurement software was written in various versions of LabVIEW. Therefore, it cannot be documented in print. Binary data files were transcribed into ASCII, and evaluated mainly using the application software Igor from Wavemetrics.

3.2 Resistor samples

After introducing the geometry of the resistor samples, we will go through the different kinds of current-voltage characteristics, and present our evaluation method for the quantitative analysis of the observed Coulomb blockade. Finally, we will arrive at a criterion for the onset of the Coulomb blockade. Via the Coulomb blockade, we observed a superconductor-insulator transition.

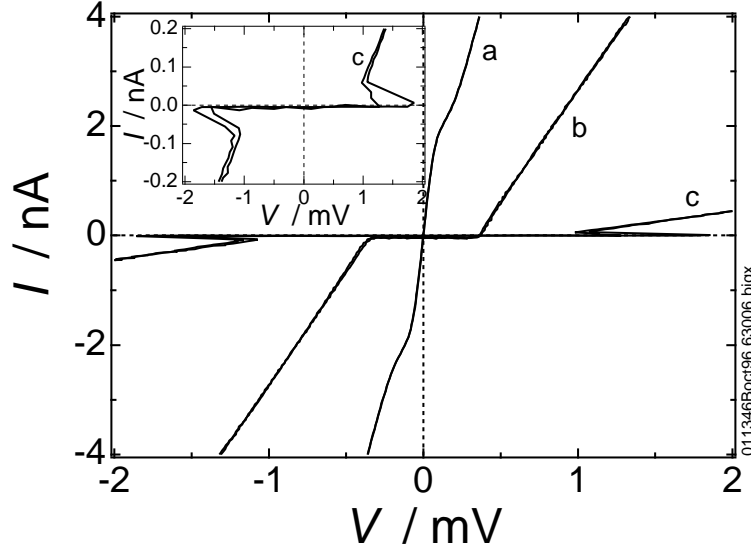


Figure 3.1: Resistor sample current voltage characteristics (IVC). For different samples with the same dimensions ($10 \times 0.15 \mu\text{m}^2$), the IVC changes with increasing sheet resistance from a supercurrent remnant (a: $1.5 \text{ k}\Omega/\square$) to a sharp Coulomb blockade (b: $8 \text{ k}\Omega/\square$). Samples with very high resistance show a back-bending IVC (c: $40 \text{ k}\Omega/\square$).

3.2.1 Sample geometry

The standard geometry for the resistor samples were strips of $10 \mu\text{m}$ length and a width limited by the lithography and pattern transfer technique in the respective state of the art, that was between 120 nm and 180 nm at the time of the resistor sample fabrication. These wires were either single, and attached to wider Nb contacts for four probe measurements, or grouped into a $120 \mu\text{m}$ long wire as in figure 2.9. These wires had probe leads spaced at $10 \mu\text{m}$ distance from each other, and resistances were also measured in four probe configuration.

3.2.2 Current-voltage characteristics

Figure 3.1 summarises the kinds of current-voltage characteristics (IVC) we observed in the resistor samples. The data presented in fig. 3.1 were taken from wires on three different chips, anodised with different times and final voltages, but with approximately equal dimensions. The measurements were taken in four probe configuration at approximately (100...200) mK in the noncommercial dilution refrigerator, and in the absence of an externally applied magnetic field.

For the most low resistive samples, like in trace (a), we found a remnant

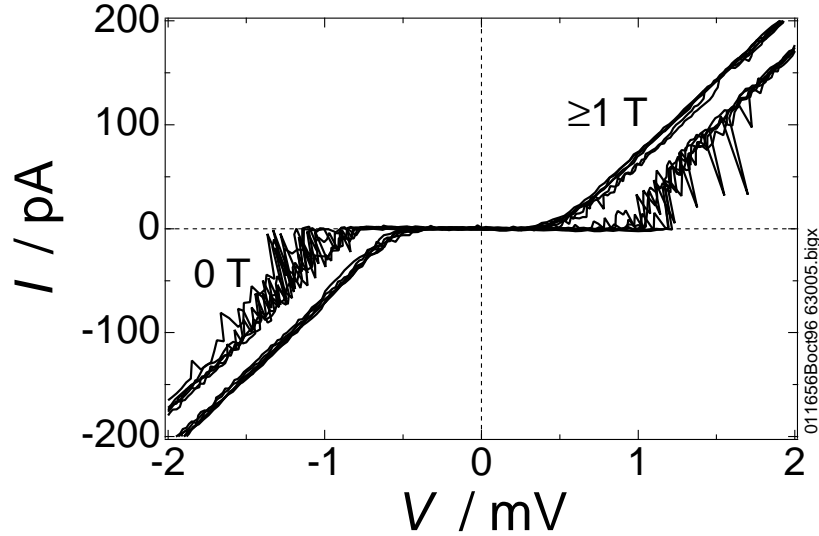


Figure 3.2: Effect of an external magnetic field on the IVC of a high resistive sample. Offset and threshold voltages are reduced, and the smoothing along the bias load line is smoothened out. Several traces superimposed for both cases.

of the supercurrent, visible as a region of reduced differential resistance up to currents of about 2 nA. This specific sample had a sheet resistance at high bias or high temperature of approximately $1.5 \text{ k}\Omega/\square$. For samples anodised deeper, we observed an increase of differential resistance around zero bias that we will from now on refer to as Coulomb blockade (justification follows in section 3.3, where we examine the samples in SET-like geometry).

Trace (b) in figure 3.1 is a typical example of a sharp Coulomb blockade with a well-defined threshold voltage. This sample had a sheet resistance of about $8 \text{ k}\Omega/\square$. In samples with very high sheet resistance, we observed not only a sharp blockade, but even a backbending of the current-voltage characteristic (trace c and inset in fig. 3.1). The backbending alone might be related to heating of the sample at the onset of current flow, where the relatively high voltage leads to high power dissipation even at low currents. On the other hand, this IVC shows a remarkable similarity with the backbending IVC observed in arrays of ultrasmall Josephson junctions by Geerligs et al. [53] and Chen et al. [54].

Another feature that has been observed in more well-defined arrays of superconducting junctions before is the switching of the current-voltage characteristics between two or more envelopes near the threshold. Figure 3.2 gives an example of such switching. The switching trace follows the load line defined by the biasing resistors. The switching is random in time and bias voltage at which it occurs in subsequent sweeps. We have observed that it suddenly settled in

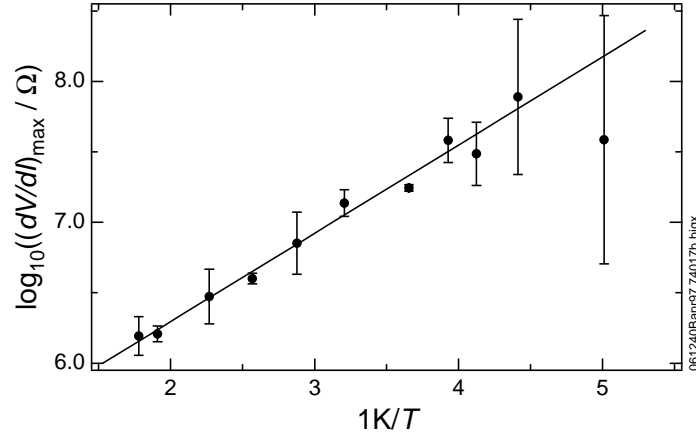


Figure 3.3: Zero bias differential resistance: temperature dependence. Determined from numerical differentiation of measured I - V curves. No magnetic field applied.

single samples some minutes after start of a measurement. The envelopes of the switching IVC seem to be reproducible, at least over a time scale of minutes. In anodised niobium samples, we have observed this switching both in the ‘old cryostat’ that had no Thermocoax high frequency filtering, and in the Oxford cryostat. These samples were not measured in the Oxford cryostat before the Thermocoax filters were installed, so that no comparison can be made in this respect. For more information on switching in a chain of Josephson junctions and the particular filtering and measuring setup, see the article by Haviland et al. [101].

Another indication for a correlation between the switching of the IVC and superconductivity is evident from fig. 3.2: here we applied a magnetic field to quench superconductivity. The switching is smoothed out, and the threshold voltage as well as the offset voltage are reduced. This behaviour saturates below 1.0 T. Shown in the figure are traces for external fields of (1.0 and 1.4) T, that coincide within the measurement accuracy. The threshold voltage is approximately reduced by a factor of two, which suggests that we might be observing the Coulomb blockade of Cooper pair tunnelling evolving into the Coulomb blockade for electrons.

The temperature dependence of the resistance is the usual criterion for classifying a material as insulating or having a superconducting transition. Our samples have quite nonlinear IVC, so that assigning a ‘global’ resistance is rather futile. Instead, one often considers the differential resistance at zero bias. A dedicated measurement would involve a careful biasing scheme and a sensitive detection, possibly involving lock-in techniques [86]. One can however, albeit

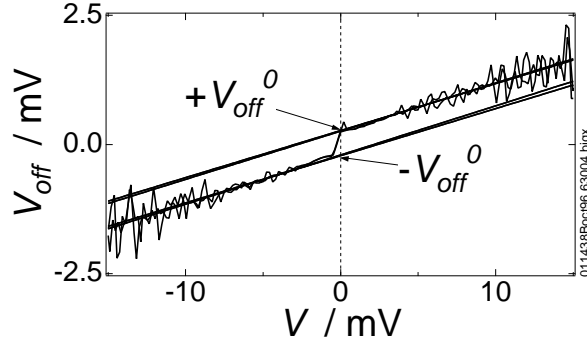


Figure 3.4: Offset voltage. Extrapolation of $V_{off}(V)$, calculated from the tangent to the $I(V)$ curve, to zero bias gives V_{off}^0 , a measure for the Coulomb blockade.

with a substantial loss of accuracy, extract some information about temperature dependence from the measured IVC. The data plotted in figure 3.3 are taken from numerically differentiated IVC. The centered value gives the height of the differential resistivity peak around zero bias, and the errors were estimated from the curvature of this peak at the centre. For an intermediate temperature range, where the Coulomb blockade is not fully developed, we see that the zero bias resistivity follows an Arrhenius law,

$$R_0(T) = R^* \cdot \exp\left(\frac{E_a}{k_B T}\right), \quad (3.1)$$

suggesting a thermally activated behaviour [86].

From figure 3.3, we extract an activation energy corresponding to a temperature of about 0.6 K or a voltage of $50 \mu\text{eV}$. This is the same order of magnitude as the voltage swing and the temperature of disappearing voltage swing in our samples in single electron transistor-like geometry, see 3.3.4. More quantitative statements are complicated since this sample might have been inhomogeneous on the length scale of micrometres due to a skewed anodisation voltage profile. The average square resistance was only about $4 \text{ k}\Omega/\square$ (total resistance $200 \text{ k}\Omega$, dimensions $10 \times 0.2 \mu\text{m}^2$), which should not have led to such a pronounced blockade according to our other measurements, and which confirms the suspicion of an inhomogeneous profile. The measurements were done in the absence of an externally applied magnetic field.

3.2.3 Measuring the Coulomb blockade: the offset voltage

Analysis of the IVC taken on our resistor samples show that they are nonlinear over many decades in bias voltage. Therefore, the offset voltage cannot simply

be determined by extrapolating the tangent to the IVC in whatever happens to be the edge of the particular measurement interval. Instead, we follow the approach by Wahlgren et al. [42], who has shown the value of an offset voltage analysis for the understanding of the Coulomb blockade.

The offset voltage V_{off} is treated as a quantity depending on the bias voltage V , and computed numerically by extrapolating the tangent to the $I(V)$ curve to the intersection with the voltage axis,

$$V_{off}(V) = V - I(V) \left. \frac{dV'}{dI} \right|_V. \quad (3.2)$$

Figure 3.4 shows the result of such a calculation. We see that V_{off} around zero bias is approximately a linear function with an offset (so, it's not linear in the mathematical meaning of the word). It is therefore possible to extrapolate the $V_{off}(V)$ curve to zero bias, and the value at the intersection with the V_{off} axis, that we denote V_{off}^0 , is well defined. This value has been shown to be of particular interest in the case of the Coulomb blockade in single junctions. V_{off} gives the limit for the blockade in the so-called 'global rule' for low environment impedances, where the whole electromagnetic environment influences the Coulomb blockade [41].

We performed four independent determinations of V_{off}^0 per IVC, namely for negative and positive voltages, and for both directions of the bias sweep.

3.2.4 Onset of the CB: a superconductor-insulator transition

Figure 3.5 shows the results of such an offset voltage analysis for a set of 187 strips from four different chips with length between $(10 \text{ and } 120) \mu\text{m}$. The errors have been estimated as the standard deviation of the four mentioned extrapolations per current-voltage characteristic.

The correlation between extrapolated zero bias offset voltage and sample resistance is obvious here where both quantities are normalised to the number of squares in the film and plotted against each other. The Coulomb blockade is appreciable for all samples with a sheet resistance larger than $10 \text{ k}\Omega/\square$, and orders of magnitude less for samples with less than $5 \text{ k}\Omega/\square$. In the intermediate region, there's a lot of clutter due to the measurement errors, and possibly some uncertainty in determining the sheet resistance. The sample width was estimated based on scanning electron microscope inspection of samples produced under similar conditions, and errors in square number determination not indicated in fig. 3.5 might very well be 20%. In any case, the Coulomb blockade sets in at a value around $6 \text{ k}\Omega/\square$. It is obvious that we observed a superconductor-insulator transition here, just in an unconventional way. While 'normally' the temperature dependence of the resistance is considered, we looked at the magnitude of the Coulomb blockade. Of course, this method per se cannot distinguish between superconducting and normalconducting behaviour, so this information has to be derived from the complete current-voltage characteristics.

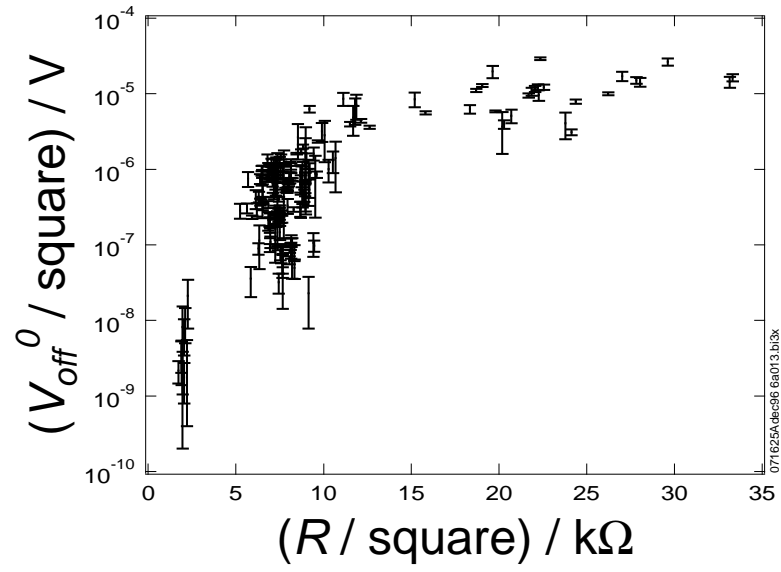


Figure 3.5: Onset of Coulomb blockade (CB) in resistor samples. Both V_{off}^0 and the sample resistance R are normalised to the number of squares in the thin film samples. The CB is clearly suppressed below $6 \text{ k}\Omega/\square$. Error bars indicate the standard deviation of four extrapolations for each set of data.

It has been suggested from studies on ultrathin metal films [60, 59] that there should be a universal sheet resistance for the superconductor-insulator transition in such films, and that it should be a fourth of the Klitzing resistance, namely the so-called ‘superconducting quantum resistance’

$$R_Q = R_K/4 = h/(4e^2) \approx 6.4 \text{ k}\Omega. \quad (3.3)$$

Values that agree with this one at least by order of magnitude, often much better though, have not only been found in studies of quench-condensed amorphous films [57, 58, 55], but also in regular arrays of ultrasmall Josephson junctions [53, 54, 102].

Our samples are obviously not regular arrays of Josephson junctions, and not homogeneous, but granular. The average grain size is supposedly a few nanometres, estimated based on the futile attempts to see grains in the scanning electron microscope and on literature data [69]. The superconducting coherence length, on the other hand, should be around 40 nm for good Nb [13]. In this case, the distinction between homogeneous and granular films should vanish [59].

3.3 Samples in SET-like geometry

We put top gates on our resistor samples and found no modulation of the IVC within the measurement accuracy. In the samples in single electron transistor-like geometry, we were more successful.

This is not surprising, if we assume that the samples should behave like arrays of very small Josephson junctions (Josephson junction arrays, JJA). A modulation of the current-voltage characteristics with a gate voltage (‘gate modulation’) occurs when the number of islands involved is small, especially when the transport properties are dominated by a single island. Chandrasekhar et al. [103, 104] found charging effects in rather short wires ($0.75 \mu\text{m}$) of $\text{In}_2\text{O}_{3-x}$. This material showed ‘the presence of large crystal grains’ [103], and the authors concluded that ‘only one or perhaps two segments (...) [were] present’ in their samples.

On the other hand, the serration of the niobium metal’s interface to the (anodic) oxide film occurs on a length scale from below one nanometre up to a few nanometres [69], so that all large grains in our thin films should have been cracked, and the sample should resemble an (irregular) array of very many junctions.

3.3.1 Current-voltage characteristics

Practically all SET-like samples showed a Coulomb blockade at millikelvin temperatures. Often this Coulomb blockade manifested itself in a hardly perceptible dip in the differential conductivity. In other samples, we observed a rather sharp Coulomb blockade, and in several samples even at liquid helium temperature,

but in none of these cases did we manage to modulate the current-voltage characteristics with an applied gate voltage. Scanning microscope inspection of these samples often suggested that there might have been a severe asymmetry between the two weak links, either by damages to the bridge during evaporation or for example by cracks in the bridge patched during evaporation. So it is quite possible that we had often produced samples that behaved more like a single junction than like a single electron transistor, and single junctions show no gate modulation of the IVC.

The samples whose IVC were susceptible to modulation by a gate voltage had more complicated IVC, like in figure 3.6. We plot the differential conductivity here since the Coulomb blockade was weak, and see a complicated system of conductivity peaks and dips around zero bias. We applied a magnetic field, and these peaks and dips moved toward zero bias. The differentiated IVC for vanishing, intermediate, and high magnetic field are given in fig. 3.6. The highest (in bias voltage) differential conductivity peaks and dips were easily identified, and in figure 3.7 their location is plotted as a function of the applied magnetic field.

At a field of 1.4 T, all structures had disappeared except for a dip in dI/dV at zero bias. This dip obviously indicates the Coulomb blockade of single electrons after the superconductivity has been completely suppressed. The interpretation of the off-zero bias structures is more complicated. The fact that they move continuously to zero bias with magnetic field suggests that they are associated with the superconducting energy gap.

3.3.2 Control curves

To see the response of the sample's current-voltage characteristic, we biased it at a series of practically constant currents and swept the gate voltage up and down with a frequency of about 8 mHz. The voltage between drain and source was registered in the usual way via the low noise amplifiers in the cryostat top box. The gate voltage was calculated from the voltage delivered from the gate voltage source and the known division factors of the respective voltage dividers in use. The design of the chip and the measurement wiring allowed to verify the presence of the gate voltage on the chip through high frequency coaxial leads.

Figure 3.8 gives a series of V_{ds} - V_g characteristics, that we refer to as 'control curves', for the sample whose differential current-voltage characteristics we examined in the previous subsection. For this measurement, all superconducting effects had been suppressed by applying an external magnetic field of 2 T.

The causal influence of the gate voltage is obvious. The control curves are far from the nice sine curves a single electron transistor would give, but the correlation between the two sweep directions in gate voltage is perceptible. The period of the voltage oscillations is of the order of 50 mV in gate voltage. If we treated the sample as a single electron transistor, this would correspond to a total island capacitance of the order of only 3 aF. This is unrealistically low if we assume that the charge of the middle island is modulated.

Control curves with such a large periodicity are, however, typical for systems

of multiple tunnel junctions [105]. Periods of several V have been observed in highly resistive superconducting microbridges [106, 107]. A serial coupling of junctions made by the step-edge cutoff technique [108] also gave a large periodicity in gate voltage [109]. Another system that has similar transport properties are nanofabricated silicon wires [110].

3.3.3 Gate modulated IVC

In one of the earliest papers on measurements on single electron devices [23], Fulton and Dolan introduced a technique of demonstrating the influence of a gate voltage on electronic transport. If one sweeps the bias voltage slowly and simultaneously the gate voltage with a higher frequency, the result is a trace zigzagging around the unmodulated current-voltage characteristic. This technique allows mapping out the entire modulation range with a single measurement.

Figure 3.9 gives the result of such a measurement on one of the samples in single electron transistor-like geometry. Here the bias was swept with a frequency of approximately 8 mHz, and the gate voltage with a frequency of 322.4 mHz and an amplitude (peak-to-peak) of 120 mV. The measurement is part of a series where the gate amplitude was up to 240 mV, but at 120 mV, the IVC were already modulated over the maximum range.

In some samples, we observed an artefact created by capacitive pickup rather than a modulation of the IVC. To ensure that the observation plotted in fig. 3.9 is not such an artefact, we checked that the amplitude of the modulation did not depend on the frequency of the gate voltage variation, at least not for frequencies of (80, 322.4 and 800) mHz. Secondly, we made sure that the deviation from the unmodulated IVC (right panel in fig. 3.9) followed the gate signal shape for sine, triangle, and square shape. In the case of IVC variations generated by capacitive pickup, the deviation followed the time derivative of the gate signal, creating spikes in the case of triangle and especially square shaped gate voltages.

Of course it would have been nice to map out the modulation range to higher bias voltages, to see it decrease again, presumably (though not necessarily). Unfortunately, this particularly nice sample was destroyed before such a measurement could be performed.

3.3.4 Temperature dependence

The temperature dependence of the gate modulation should give information about the energy scale on which the Coulomb blockade occurs. In the following, we present the results of the temperature dependent measurements of the sample from figure 3.9. The available data are sufficient to allow some comparison with single electron transistors reported in the literature.

Figure 3.10 proves that the Coulomb blockade and its modulation by the gate voltage persisted at temperatures above 1 K. The data were taken with the same method as that in figure 3.9. The unmodulated current-voltage characteristic was taken a few minutes before the modulated one. In the meantime,

it had switched to another trace, so that the difference between modulated and unmodulated IVC, the voltage swing, is not symmetric around zero. Such a switching occurred every few minutes, and is a well-known phenomenon in single electron transistors.

Most probable cause for the switching between several IVC is a change in the configuration of the (random) background charge near the transistor active structure. Background charge is an important contributor to noise in single electron transistors. Oxides, like the barrier oxide or an oxidised substrate, are a source of randomly fluctuating background charges and thus of noise. In this respect, niobium resistors may be rather disadvantageous, since they inevitably contain large amounts of oxides.

The temperature dependence of the voltage swing is shown in figure 3.11. For the low temperature values up to 600 mK, the swing ΔV was analysed in the bias region between -7.5 nA and 7.5 nA, and the root-mean-square value of the amplitude is plotted together with some estimate of the uncertainty, versus the temperature. Errors in the temperature measurement were negligible on this scale. The high temperature at 1130 mK in figure 3.11 was determined by comparison of the amplitudes of the voltage swing at ± 7.5 nA in two measurements with a square shaped gate modulation and normalised to the low temperature amplitude.

As expected, the amplitude of the modulation decreases with temperature. A simple extrapolation of the few data points in figure 3.11 gives a temperature value between 2 K and 3 K where the voltage swing vanishes and which we denote as T^* . The peak-to-peak maximum voltage swing found for this sample at low temperature was at least 100 mK; it might have been somewhat bigger, if one had been able to measure on this sample at higher bias. This corresponds to a temperature of about 1.2 K, or about one half T^* .

For single electron transistors made by angular evaporation, Wahlgren [111] found an approximate relation

$$e\Delta V_{max} \approx 4k_B T^*. \quad (3.4)$$

This relation seems to hold even for the very small single electron transistors made by Nakamura et al. [112] that had a T^* of the order of 100 K. In both these cases, the junction resistances were considerably above the quantum resistance R_K .

Our sample considered above, on the other hand, had a total resistance of less than R_K . In such low-resistive samples, cotunnelling plays an important role, that is the ‘simultaneous’ tunnelling through a virtual state between two tunnel barriers. Cotunnelling could account for the reduction of the voltage swing compared to the ‘ideal’ single electron transistor described by (3.4).

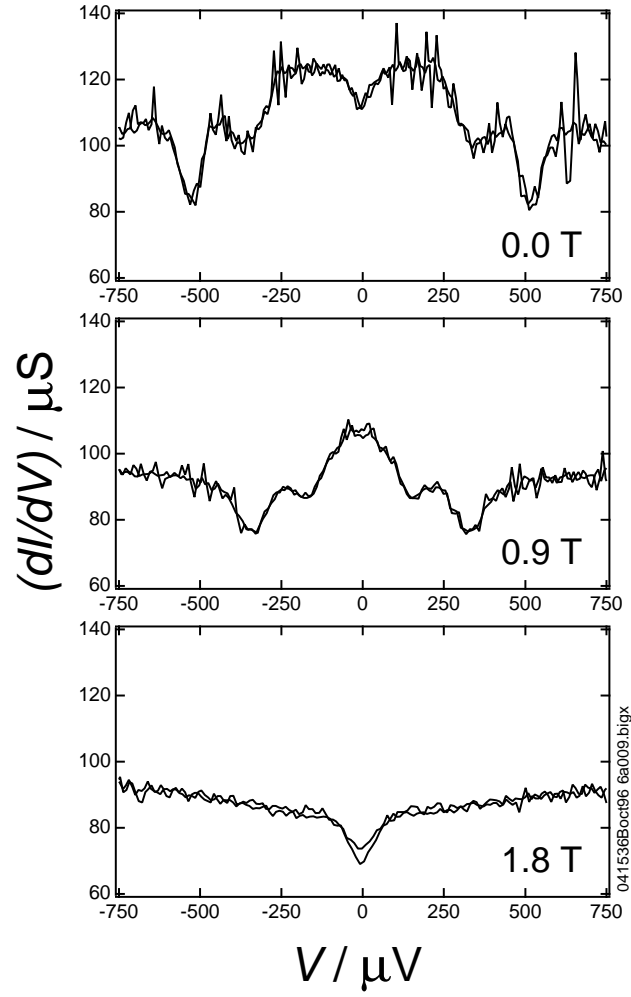


Figure 3.6: Coulomb blockade in a sample with two anodised weak links in SET geometry. As superconductivity is squeezed by external magnetic fields, the off-zero-bias differential conductance peaks disappear, and a Coulomb blockade for electrons remains.

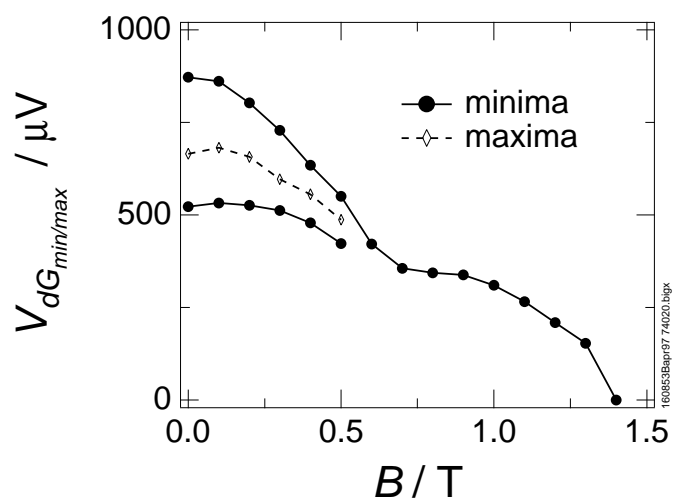


Figure 3.7: Magnetic field dependence of differential conductance minima and maxima in figure 3.6. Values have been averaged from the positive and negative voltage semiaxes. Lines are to guide the eye.

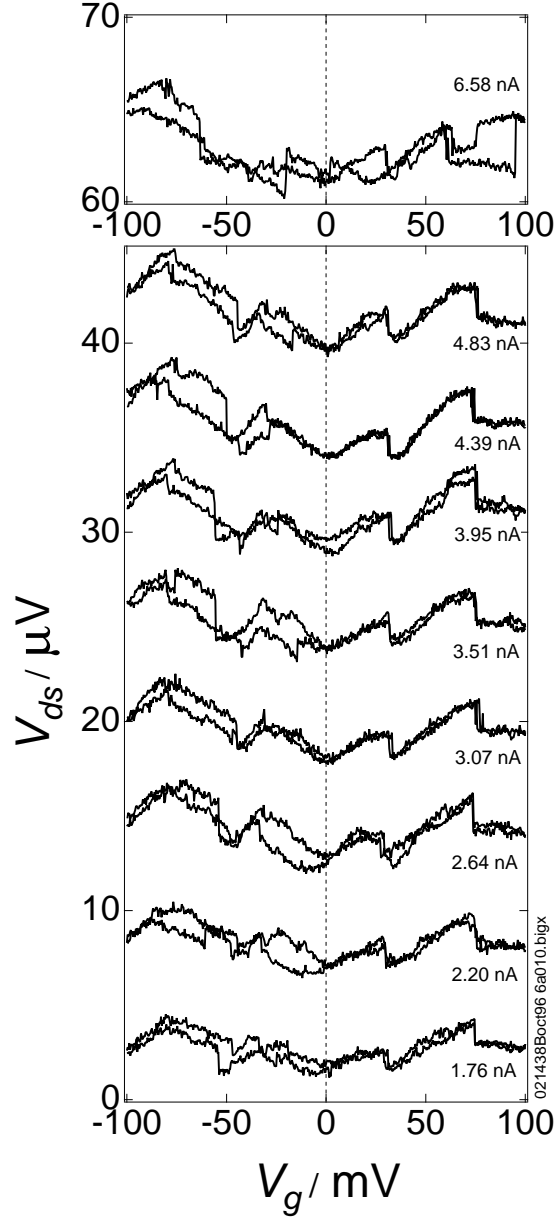


Figure 3.8: Control curves for a sample with two anodised weak links in SET geometry. The drain-source voltage V_{ds} (at different current bias points) oscillates as the voltage V_g applied to a top gate is swept up and down.

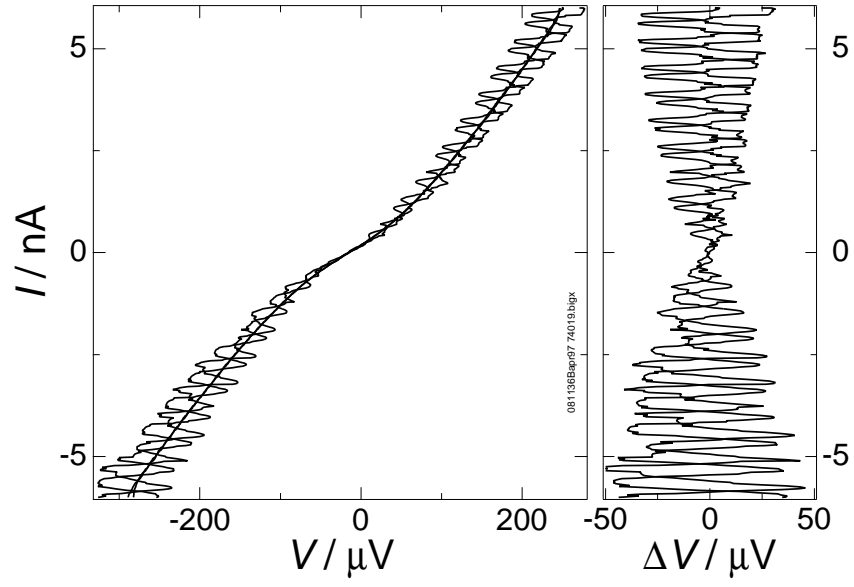


Figure 3.9: Gate modulated I - V characteristics. The gate voltage was modulated with 40 times the frequency of the bias sweep (bias was ramped up and down once). Left: resulting I - V curve (wavy) and IVC in the absence of a gate voltage (straight). Right: voltage swing ΔV , defined as the difference between modulated and unmodulated IVC. $T \approx 50$ mK, no external magnetic field.

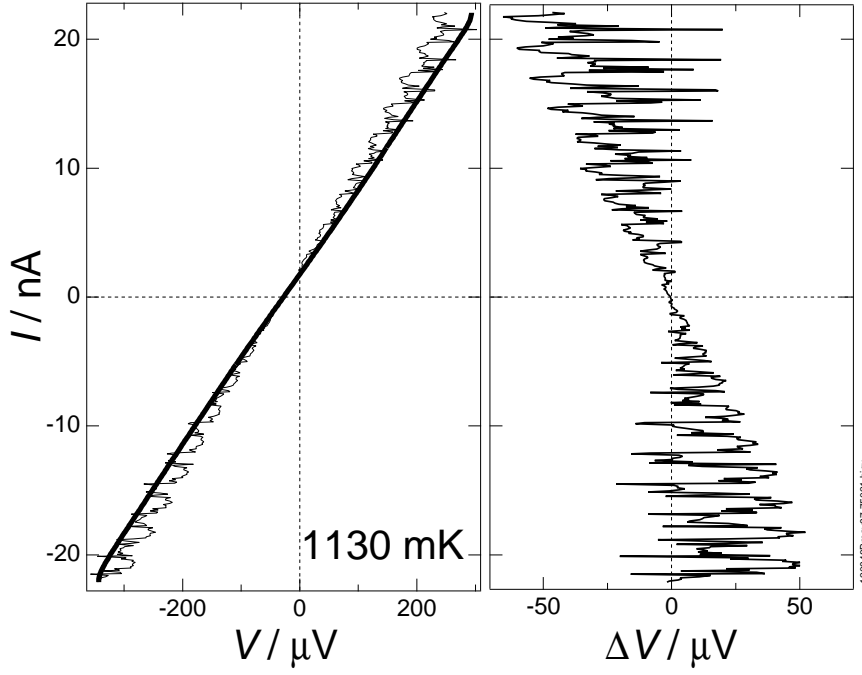


Figure 3.10: Modulation of the IVC with gate voltage (cf. fig. 3.9), at a temperature of (1130 ± 10) mK. Only one direction of the bias ramping is shown here. The thick trace in the left panel is an unmodulated IVC taken a few minutes earlier, ΔV the difference to that IVC. Gate voltage amplitude $V_{pp} = 200$ mV.

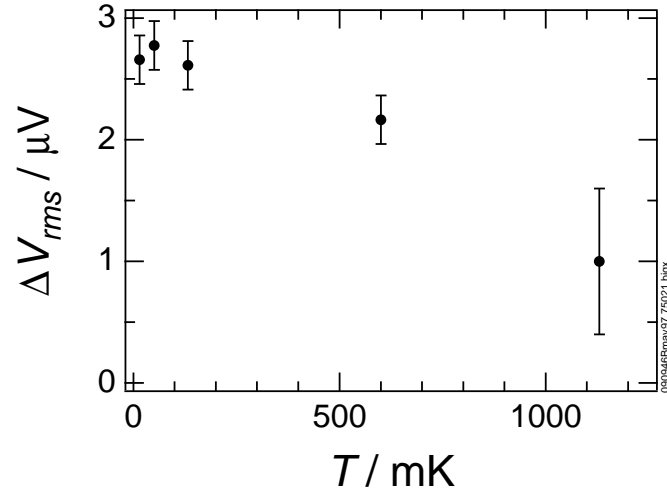


Figure 3.11: Temperature dependence of the voltage swing for the sample from figs. 3.9 and 3.10. The first four values have been obtained from an analysis of a calculation of the rms amplitude in the bias region $(-7.5 \dots 7.5)$ nA for sine shaped gate modulation, the last value by comparison of amplitudes at the edges of this region for a square shaped modulation. The error bars indicate a rough estimate.

Chapter 4

Conclusion

4.1 Status quo

We have successfully adapted and developed methods for the fabrication of high-ohmic low-capacitance resistors. By means of anodic oxidation, these resistors can be trimmed with a spread in resistance values of less than 10% for a value of a few hundred k Ω on the length of a few tens of micrometres. There is no need to monitor and anodise each resistor independently; however, one monitored resistor per anodisation process is required since the resistance depends sensitively on film thickness, and on anodisation voltage and time in a way far too complex to allow a prediction based trimming.

We have found that our nanofabricated resistors showed nonlinear current-voltage characteristics, with a transition from superconducting behaviour to a Coulomb blockade with increasing sheet resistance. A purely ohmic behaviour is practically impossible to achieve, though one might suppress the supercurrent with a magnetic field. But even in this case, a (weak) Coulomb blockade remained. The Coulomb blockade grew by orders of magnitude when the sheet resistance of the films exceeded a value that seems to agree with the quantum resistance for Cooper pairs $R_K/4 \approx 6.45$ k Ω .

We have fabricated a device based on two weak links in a niobium thin film strip, defined by shadow evaporation and anodisation, in a geometry resembling that of a single electron transistor. These samples could be equipped with an overlapping gate thanks to the insulating properties of the anodic oxide film. By applying a voltage to the gate, the conductance of the device could be modulated.

The behaviour resembled closely that of a single electron transistor, but the shape of the control curves suggests that we were in fact dealing with multiple tunnel junctions in 100 nm wide structures. A further reduction of size seems hard to achieve; however, changes in design might alleviate the problem of asymmetry between the junction arrays on both sides of the transistor island.

For low resistive, transistor-like samples, a suppression of the voltage mod-

ulation compared to single electron transistors was found that can be explained by cotunnelling. Due to the multiple junction nature of the weak links, there is a tradeoff between a tendency to a more gate controllable blockade at lower resistance (because fewer junctions are involved), and the weakening of this blockade due to cotunnelling (for the same reason).

4.2 Directions for future research

The superconductor-insulator transition should be investigated with samples in different (wider) geometry to corroborate the found dependence of the Coulomb blockade on the sheet resistance. Temperature and magnetic field dependent data on the superconductor-insulator transition are needed. With the four layer resist technique presented above, however, results would have been compromised by the grainy surface contamination occurring on large exposed surfaces. First tests with three layer resist (PMMA-Ge-PMGI) are very promising for the fabrication of structures from 100 nm to many micrometres without surface contamination. Therefore, this technique would also enable the fabrication of well-defined junction arrays for comparative studies. Prerequisite is the availability of good e-beam evaporated niobium, and test runs of a new niobium evaporation system (April 1997) indicate that we can now make Nb thin films with transition temperature close to the bulk value in 100 nm thick films.

It remains to use anodisation fabricated niobium thin film resistors for the purpose they were originally intended for, namely as biasing resistors for ultra-small tunnel junctions, in an attempt to learn more about the interplay of the Coulomb blockade and the electromagnetic environment.

The single electron transistor-like samples should be made with an improved fabrication process, and characterised systematically by magnetic field dependent and especially temperature dependent measurements.

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Appendix A

Symbols and notation

Table A.1: Meaning, SI unit and numerical value [113] (if applicable) of symbols used in this report

Symbol	meaning (numerical value)	SI unit
Δ	superconducting energy gap	$\text{m}^2 \text{kg s}^{-2}$
ΔV	voltage swing (modulation)	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
γ	phase difference over Josephson junction	1
ε	relative dielectric permittivity	1
ε_0	dielectric permittivity of vacuum ($8.854 \dots \cdot 10^{-12}$)	$\text{m}^{-3} \text{kg}^{-1} \text{s}^4 \text{A}^2$
λ	London penetration depth	m
μ_0	permeability of vacuum ($1.256 \dots \cdot 10^{-6}$)	$\text{m kg s}^{-2} \text{A}^{-2}$
ξ	coherence length	m
ϱ	density	$\text{m}^{-3} \text{kg}$
ϕ	phase of multiparticle wavefunction	1
A	area	m^2
B	magnetic flux density	$\text{kg s}^{-2} \text{A}^{-1}$
C	capacitance	$\text{m}^{-2} \text{kg}^{-1} \text{s}^4 \text{A}^2$
d	thickness	m
e	elementary charge ($1.602 \dots \cdot 10^{-19}$)	s A
E	energy	$\text{m}^2 \text{kg s}^{-2}$
E_a	activation energy	$\text{m}^2 \text{kg s}^{-2}$
E_C	characteristic charging energy $e^2/(2C)$	$\text{m}^2 \text{kg s}^{-2}$
E_{ch}	charging energy	$\text{m}^2 \text{kg s}^{-2}$

Symbol	meaning (numerical value)	SI unit
E_J	Josephson (coupling) energy	$\text{m}^2 \text{kg s}^{-2}$
G	conductivity	$\text{m}^{-2} \text{kg}^{-1} \text{s}^3 \text{A}^2$
H	magnetic field	$\text{m}^{-1} \text{A}$
h	Planck's constant ($6.626 \dots \cdot 10^{-34}$)	$\text{m}^2 \text{kg s}^{-1}$
\hbar	Planck's constant divided by 2π ($1.054 \dots \cdot 10^{-34}$)	$\text{m}^2 \text{kg s}^{-1}$
I	current	A
I_c	critical current	A
I_{c0}	maximum critical current	A
I_s	supercurrent	A
k_B	Boltzmann constant ($1.380 \dots \cdot 10^{-23}$)	$\text{m}^2 \text{kg s}^{-2} \text{K}^{-1}$
l	length	m
Q	charge	s A
R	resistance	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-2}$
R_K	quantum resistance	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-2}$
R_{K-90}	Klitzing resistance (25812.807)	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-2}$
R_Q	'quantum resistance for pairs' $R_K/4$	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-2}$
R_T	tunnelling resistance	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-2}$
t	time	s
T	temperature	K
T^*	temperature at which voltage swing vanishes	K
T_c	critical temperature	K
V	voltage	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
V_{off}	offset voltage	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
V_{off}^0	(extrapolated) zero bias offset voltage	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
x	spatial coordinate	m

Appendix B

Glossary and abbreviations

Ångström (Å): Outdated unit of length. $1 \text{ Å} = 10^{-10} \text{ m}$.

ACME: Anodization controlled miniaturization enhancement [83]

AF: Anodic film (more general than AOF, may incorporate inclusions from the electrolyte)

Ammonium pentaborate: $(\text{NH}_4)\text{B}_5\text{O}_8 \cdot x\text{H}_2\text{O}$ [114], where x indicates the amount of crystal water. If undefined, we assume $x \approx 4$ (APB tetrahydrate).

AOF: Anodic oxide film

APB: Ammonium pentaborate

ASCII: American Standard Code for Information Interchange

CAD: Computer Aided Design

Cb: Chemical symbol for Columbium

CB: Coulomb blockade

CBCPT: Coulomb blockade of Cooper pair tunnelling

CHET: Charging effect transistor

Chip marks: Alignment marks (JEOL EBL system) used for highest precision alignment. Three chip marks have to be situated within one field. In the work described here, wafer marks were used instead.

Columbium (Cb): old name for Niobium (Nb), used in the Angloamerican language space until about 1950 and in the American metallurgical community even later.

Contrast: Degree to which the physicochemical properties exploited in resist development differ in exposed areas compared to unexposed areas

CP: Copolymer P(MMA-MAA)

DAQ: Data acquisition

DMM: Digital multimeter

DMS: Dilute magnetic semiconductor

DXF: Drawing Exchange Format

DVM: Digital voltmeter

ECU: European currency unit

EBL: Electron beam lithography

EOS: Electron optical system

Field: Area that can be written by the EBL without the need of moving the stage, $80 \times 80 \mu\text{m}^2$ in highest resolution mode. At the edges of the fields, stitching error occurs, so fine structures should not cross field boundaries.

Forming: The process of growing an anodic [oxide] film

Gauss (G): Hopelessly outdated unit of magnetic flux density in one of the various CGS systems. Corresponds to (but is not equal to) 0.1 mT.

GDS-II: Stream format, a.k.a. Calma Stream. The industry standard for lithographic pattern data.

GPB: General purpose interface bus (IEEE-488)

IBE: Ion beam etching (milling)

Inch: Outdated unit of length. 1 in = 25.4 mm

IUPAC: International Union of Pure and Applied Chemistry

IVC: Current-voltage characteristic

JEOL: Japanese manufacturer of electron optical research instrumentation

JJ: Josephson junction

JJA: Josephson junction array

Jobdeck file (JDF): Text file in the JEOL EXPRESS system that describes which patterns (chips) are to be exposed and where they are to be positioned relative to each other, and that contains the definition of the shot modulation and the alignment (mark detection) parameters. It also points to a calibration sequence of the electron optical system that will be carried out at the beginning of the exposure and eventually during the exposure.

Microfabrication: Fabrication of devices with typical linear dimensions below $1\text{ }\mu\text{m}$

M-IT: Metal-insulator transition

ML: Monolayer

Nanofabrication: The art and science of producing non-random structures with typical linear dimensions less than 100 nm

Negative resist: Resist that is removed during development where it has *not* been exposed. Example is SAL 601 (e-beam resist).

PMGI: Poly(dimethyl glutarimide), a positive e-beam and deep UV resist

PMMA: Polymethylmethacrylate, a positive e-beam resist

P(MMA-MAA): Copolymer poly(methylmethacrylate-methacrylic acid), a positive e-beam resist, more sensitive than PMMA

Positive resist: Resist that is removed during development where it has been exposed. Examples are PMMA (e-beam resist) or S-1813 (photoresist).

PROXECCO: A commercial computer programme for proximity correction [88].

Proximity correction: Increasing the exposure dose for narrow and/or isolated features to compensate for the proximity effect.

Proximity effect: Additional exposure of pixels with many neighbouring exposed pixels due to scattering of the electron beam in the resist and substrate and to secondary electrons.

QPT: Quantum phase transition

RIE: Reactive ion etching

Rotation: Angular misorientation of the sample relative to the sample holder and consequently the whole electron beam lithography machine. Rotation has to be compensated by the EOS, increasing inaccuracies (stitching error) and pattern distortions. A limit on allowed rotation is set in the internal configuration files of the JEOL system.

RRR: Residual resistance ratio, between the resistances at room temperature and just above the resistive transition or at 4.2 K; a measure for the quality often used for Nb.

S-1813: A positive photoresist

SAL 101: A developer for PMGI

SAL 601: A negative e-beam resist

Schedule file (SDF): Text file in the JEOL EXPRESS system that describes where the arrangement of patterns defined in the jobdeck file is to be placed relative to the machine and what the reference dose for the shot modulation is. It also contains information on hardware settings and definitions for the alignment mark detection.

Selectivity: Ratio of the solubilities of different resists exposed simultaneously, important for the resolution in processes involving two layer resist systems

SEM: Scanning electron microscope

Sensitivity: Reciprocal of the irradiation dose required to produce the physicochemical modifications in a resist needed for development

SET: Single electron tunnelling, alt. single electron (tunnelling) transistor

Shadow evaporation technique: also known as Dolan technique, Niemeyer-Dolan technique, nonvertical evaporation technique etc. A method of forming very small overlap junctions in the shadowed area underneath a suspended bridge on the substrate. Self-aligning, involves only one lithography step. Introduced by Niemeyer [84], in its present form with resist mask by Dolan [85].

Shot modulation: JEOL-specific implementation of handling the assignment of doses to pattern parts (to compensate the proximity effect). Each primitive is assigned a shot rank (an integer number) that corresponds to a certain dose enhancement factor (a floating point number). This assignment is called the shot modulation.

S-IT: Superconductor-insulator transition

SNAP: Selective niobium anodization process [77]

SnL: Swedish Nanometre Laboratory, Göteborg.

Stitching error: Misalignment of parts of the electron beam exposed pattern at the boundaries of fields and subfields. Stitching error increases with sample rotation.

Subfield: Area that can be written by the EBL without switching digital-to-analogue converters, $10 \times 10 \mu\text{m}^2$ in highest resolution mode. At subfield boundaries, slight stitching error occurs, so the finest nanostructures should not cross them.

Tear-off technique: A special form of angular evaporation technique where some material is deposited on resist sidewalls and removed during liftoff. Requires good control over the undercut and the evaporation angles.

TEM: Transmission electron microscopy

UHV: Ultra high vacuum, below 10^{-6} Pa

Vector scan: EBL mode where the beam is swept only over the areas that are to be exposed, as opposed to raster scan, where it is swept over the whole sample and simply blanked from non-exposure areas. Requires faster electron optics and makes systems more expensive, but can save a lot of exposure time.

VTB: Variable thickness bridge

Wafer marks: Alignment marks (JEOL EBL system) that can be placed almost anywhere on the sample. Of course, precision of alignment improves when the marks are as close to the writing area as possible.

ZEP 520: A positive e-beam resist

Appendix C

Recipes

All recipes assume that reactive ion etching (RIE) is done in a Plasmatherm Batchtop 70 with a seven inch electrode (area 248 cm^2), an electrode distance of 60 mm and a working frequency of 13.56 MHz.

The contact printer operates in the wavelength range $(320 \dots 420)\text{ nm}^2$.

Electron beam lithography was done with a JEOL JBX 5D-II system with CeB_6 cathode.

C.1 Photomask making

1. Rinse a Cr mask with deionised tap water.
2. Ash the surface with oxygen RIE, pressure 33 Pa, flow $36\text{ }\mu\text{mol/s}$, rf power 50 W, time 30 s.
3. Spin Microposit Primer.
4. Spin Shipley SAL-601 at 4000 rpm, giving a thickness of about 800 nm.
5. Preexposure bake for 20 min at 90°C in an oven.
6. E-beam expose in the JEOL JBX 5D-II. Design dose $10\text{ }\mu\text{C/cm}^2$, acceleration voltage 50 kV, fourth lens (working distance 39 mm), third aperture (diameter $300\text{ }\mu\text{m}$), current 5 nA.
7. Postexposure bake for 20 min at 110°C in an oven.
8. Develop in Microposit MF322 for about 6 min, inspect in the microscope.
9. Ash the surface in the RIE (see above) and immediately thereafter
10. etch in Balzers No.4 chromium etch (composition: 200 g cerium ammonium nitrate, 35 mL 98% acetic acid, filled with deionised water to 1000 mL).

11. Remove the resist by stripping with RIE. Process gas oxygen, pressure 66 Pa, flow $7\text{ }\mu\text{mol/s}$, rf power 250 W, time 120 s.

C.2 Gold pad photolithography (carrier chips)

1. Strip the surface of an oxidised two inch Si wafer with RIE. Process gas oxygen, pressure 66 Pa, flow $7\text{ }\mu\text{mol/s}$, rf power 250 W, time 120 s.
2. Spin Shipley S-1813 at 5500 rpm, giving a thickness of about 1000 nm.
3. Bake for 7:30 min at $110\text{ }^{\circ}\text{C}$ on a hotplate.
4. Expose for 12 s at an intensity of 10 mW/cm^2 , correspondingly longer or shorter for different intensities.
5. Develop in a 1:1 mixture (by volume) of Microposit Developer and deionised water for 60 s, rinse thoroughly with deionised water from the tap.
Or:
6. Develop in pure MF 322 developer for 15 s and rinse.
7. Ash the surface with oxygen RIE, pressure 33 Pa, flow $36\text{ }\mu\text{mol/s}$, rf power 50 W, time 30 s. Immediately thereafter
8. evaporate 20 nm of $\text{Ni}_{0.6}\text{Cr}_{0.4}$ at 0.1 nm/s and
9. 80 nm Au at 0.2 nm/s .
10. Liftoff in slightly warmed acetone.
11. Presaw from the back to a depth of about $50\text{ }\mu\text{m}$. When cutting alignment edges from the front side, try to preserve a C_4 symmetric circumference shape of the wafer; this facilitates later resist preparation.

C.3 Four layer resist preparation

1. Ash the surface of a wafer with gold chip patterns with RIE. Process gas oxygen, pressure 33 Pa, flow $36\text{ }\mu\text{mol/s}$, rf power 50 W, time 30 s.
2. Spin 350k PMMA (1.8 %, in xylene) at 2500 rpm to a thickness of about 50 nm.
3. Bake for 12 min at $170\text{ }^{\circ}\text{C}$ on a hotplate.
4. Spin Shipley S-1813, diluted 1:1 by volume with Shipley P-Thinner, at 3000 rpm, giving a thickness of about 200 nm.
5. Bake for 12 min at $160\text{ }^{\circ}\text{C}$ on a hotplate.
6. Evaporate 20 nm Ge at 0.2 nm/s .

7. Spin 350k PMMA (1.8 %, in xylene) at 2500 rpm to a thickness of about 50 nm.
8. Bake for 10 min at 150 °C on a hotplate.
9. Break into suitable chip sets for further handling.

C.4 Four layer resist exposure

Acceleration voltage 50 kV, first aperture (diameter 60 μm), fifth lens (working distance 14 mm), current 20 pA for the fine patterns (1 nA for the coarser leads). Area doses

- 1120 $\mu\text{C}/\text{cm}^2$ for 20 nm wide lines.
- 400 $\mu\text{C}/\text{cm}^2$ for 100 nm wide lines.
- 280 $\mu\text{C}/\text{cm}^2$ for all wider lines and areas.

C.5 Four layer resist proximity correction

(for PROXECCO:) double Gaussian with $\alpha = 0.006 \mu\text{m}$, $\beta = 6 \mu\text{m}$ and $\eta = 0.5$. The low η is due to the Ge layer that absorbs a large fraction of the backscattered electrons. Number of doses 32, output quality fine, physical fracturing.

C.6 Four layer resist processing

1. Expose in the EBL machine (see C.4).
2. Develop in a mixture of 10 volume parts isopropanole and 1 volume part deionised water for 60 s under ultrasonic excitation.
3. Reactive ion etching: pattern transfer to the Ge mask. Process gas CF_4 , pressure 1.3 Pa, flow 7.5 $\mu\text{mol/s}$, rf power 14 W, time 120 s.
4. RIE of the support layers. Process gas O_2 , pressure 13 Pa, flow 15 $\mu\text{mol/s}$, rf power 20 W, time 15 min.
5. Evaporate Nb with e-gun heating. Deposition rate about 0.5 nm/s.
6. Liftoff in slightly warmed acetone, spraying chip centres directly with a syringe.

C.7 Anodisation window mask

1. Spin 950k PMMA (8 %, in chlorobenzene) at 5000 rpm, giving a thickness of about $1.8\text{ }\mu\text{m}$.
2. Bake for 12 min at 170°C on a hotplate.
3. E-beam expose with an area dose of $280\text{ }\mu\text{C}/\text{cm}^2$. Acceleration voltage 50 kV, first aperture (diameter $60\text{ }\mu\text{m}$), fifth lens (working distance 14 mm), current 1 nA.
4. Develop in a mixture of 10 volume parts isopropanole and 1 volume part deionised water under ultrasonic excitation for 8 min.

C.8 Electrolyte for Nb anodisation

Downscaled from the recipe of Joynson [97]: 8.3 g ammonium pentaborate, 60 mL ethylene glycole and 40 mL distilled water to be stirred and heated to about 100°C . The solution has to be regenerated by heating and stirring before using since the ammonium pentaborate precipitates.

C.9 Two layer resist for high resolution EBL

1. Spin copolymer (6 %, in 2-ethoxy-ethanole) at 5000 rpm, to a thickness of about 140 nm.
2. Bake for 5 min at 170°C on a hotplate.
3. Spin NANO-PMMA (2 %, in anisole) at 5000 rpm, giving a film thickness of about 50 nm.
4. Bake for 5 min at 170°C on a hotplate.
5. E-beam expose.
6. Develop in a mixture of 10 volume parts isopropanole and 1 volume part deionised water under ultrasonic excitation for 50 s.

C.10 Ti dot patterns (etch mask for IBE) on II-VI semiconductors

1. Prepare two layer resist (see C.9).
2. E-beam expose with an acceleration voltage of 50 kV, first aperture (diameter $60\text{ }\mu\text{m}$), fifth lens (working distance 14 mm), current 1 nA. Dose
 - $700\text{ }\mu\text{C}/\text{cm}^2$ for $50 \times 50\text{ nm}^2$ squares on a 250 nm periodic square lattice,

- $220 \mu\text{C}/\text{cm}^2$ for $200 \times 200 \text{ nm}^2$ squares on a 400 nm periodic square lattice.
3. Develop (see C.9).
 4. Evaporate 30 nm Ti.
 5. Liftoff in warm acetone. Apply jet from a syringe needle, this may take a while.

C.11 Ar^+ ion beam milling of II-VI semiconductor quantum dots

1. Make Ti dot mask (see C.10).
2. Mill for 20 min under normal incidence. Acceleration voltage 200 V , current density $0.16 \text{ mA}/\text{cm}^2$. Etching rate under these conditions is approximately 20 nm per minute for $\text{Cd}_{1-x}\text{Mn}_x\text{Te}$.
3. Remove the Ti in 10% HF (a few seconds), rinse with water and isopropanol.

C.12 Chemical etching of II-VI semiconductor quantum dots

1. Dissolve one drop of Br_2 in 10 mL ethylene glycol.
2. Etch for half a minute.
3. Check under the SEM.
4. Repeat etch and check until satisfied.